Kaiam Corporation
Harvey Mudd College Global Clinic

# Development of a Novel Burn-In System for Micron Scale Laser Diodes


Tommy Berrueta, Evan Kahn, Jeewan Naik, Emily Schooley,
Hamza Khan, Yashas Hegde

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Professor Matthew Spencer

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Christopher Stonier, Bardia Pezeshki, Mike Jubber,
Dinh Ton, Jay Kubicky, Jacinto Dominguez

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# Abstract

Kaiam Corporation manufactures laser diodes for optical transceivers. Their manufacturing line is limited by the burn-in process for the diodes. A modular burn-in system has been developed which can test more laser diodes than Kaiam's current burn-in solution, at a lower cost. The burn-in system is comprised of an aluminum assembly, a pair of silicon wafers, and control circuitry, all contained inside of a rack mounted enclosure. The primary innovation in this system is the use of MEMS cantilevers tipped with gold solder balls to make contact with the laser diodes. The wafer containing these cantilevers, the diodes under test, and the aluminum assembly can be assembled by an MRSI die-bonder, which reduces human error when loading and unloading laser diodes. These assemblies connect to the enclosure through a custom built shorting connector, which provides ESD protection for the lasers. The system costs $52.30 per laser diode, which represents a significant reduction from the existing solution. The wafers are still being fabricated, but the rest of the burn-in system has been assembled and tested.



# Acknowledgements

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# 1 Introduction

Kaiam Corporation designs and manufactures high-speed optoelectronic transceivers for short-range fiber optic links in data centers. These transceivers are composed of millimeter-scale laser diodes which are packaged on silicon chip-on-carrier, or CoC, breakouts. The diodes convert electrical inputs from a server into optical outputs. Kaiam's transceivers operate at a higher bandwidth than the current industry standard because their modules integrate multiple optical diodes operating at different transmission frequencies.

Each diode needs to be tested at high temperature and current to ensure that the transceiver lifetime is not limited by early diode failure. This test is called "burn-in". Kaiam currently uses a custom burn-in apparatus built by a Chinese company called Yelo for this procedure.

The Harvey Mudd Kaiam Global Clinic team is tasked with developing a scalable, modular burn-in system. It must limit human interaction with the device under test to reduce technician effort and increase yield. It also needs to have a higher throughput and lower cost per diode than the Yelo system.

## 1.1 Limitations of the Yelo System

Kaiam Corporation's current system for burning-in laser diodes, the Yelo system, requires human operators to use tweezers to pick up the small CoCs, place them on a testing module, and manually lower delicate tungsten probes attached to the module to make electrical contact with the CoCs. Figure 1 shows four different views of the Yelo system.

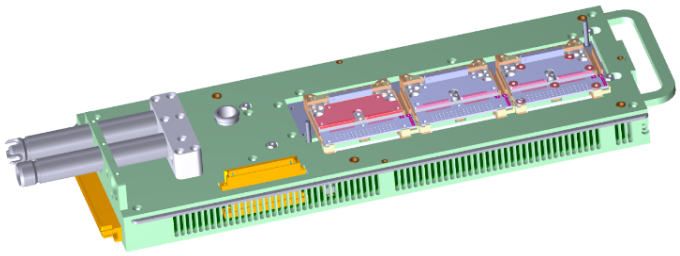
## 1.2 Proposed System

The burn-in procedure described in this document uses a robotic die bonder machine, manufactured by MRSI Systems, to arrange CoCs between two micromachined silicon wafers. The features of these wafers make both physical and electrical contact with the CoCs. The wafers are housed in an aluminium shell along with cartridge heaters, which allow the shells to reach the high temperatures required for burn-in, and circuit boards, which are used to facilitate electrical contact between the diodes and the outside world. This ensemble of parts will be referred to as the "main assembly" or "assembly". The main assembly is inserted into an enclosure, in which the burn-in is conducted. A control board is thermally isolated from the main assembly inside the enclosure. It provides power to, and communicates with, the onboard electrical components in the main assembly.

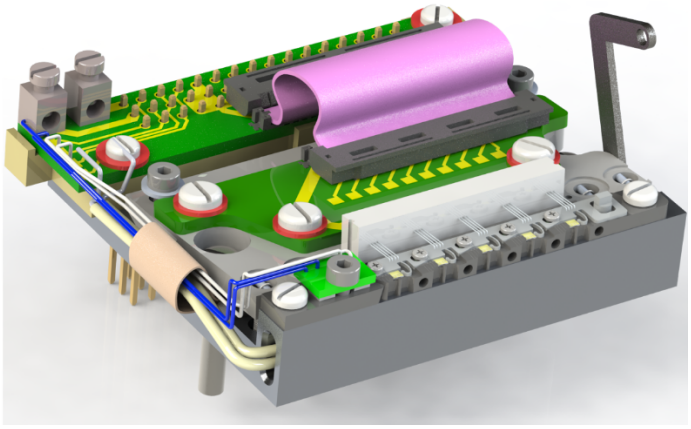
The cost of the new system was estimated to be $104.59 per CoC (see Appendix B for a detailed summary of costs). This is much lower than the $500 per CoC cost of the Yelo system. The lead time on repairs will be shorter because components of this system will be manufactured in-house or purchased off the shelf. The system is modular, so extra capacity can be added as needed.

This process, though functional, has become a bottleneck in Kaiam's manufacturing. Kaiam is currently burning-in approximately 10,000 units each week and Kaiam expects that number to increase significantly. The Yelo system is poorly positioned to match this increase in production. It requires slow, manual loading, which means that personnel costs


**(a)** Full Rack



**(b)** Modular Insert



**(c)** CoC Holder

**Figure 1:** (a) The Yelo racks that Kaiam uses for burn-in currently. The entire rack costs ∼$500,000 (b) Single tray which is slid into the rack. The dimensions are ∼40 cm by ∼15 cm. (c) Individual CoC holder with fragile tungsten probes circled. There are three of these per tray and each one can hold five CoCs.

scale with the number of devices being burned-in. It is very expensive: the cost per CoC position is approximately $500. Finally, it is unreliable: the tungsten probes on the Yelo testing module, shown in Figure 1c, are fragile, expensive, and difficult to repair. The probes break or bend if touched accidentally by an operator or lowered past a certain point, and replacing probes requires that the entire assembly be shipped to Ireland, which takes the module off the factory floor for a long time.

## 1.3 Document Organization

This report describes the system developed by the HMC Global Clinic team for Kaiam Corporation. Section 2 describes the main assembly which holds and makes electrical contact with the CoCs. Section 3 details the enclosure designed to hold the assembly and conduct the burn-in test. Section 4 reviews the control board which maintains the current through the diodes and the temperature of CoCs. Section 5 discusses the future work necessary for successful implementation of this system, including the testing necessary to verify function of the wafers and the discussion of a few minor changes that could be implemented. Section 6 concludes the report.

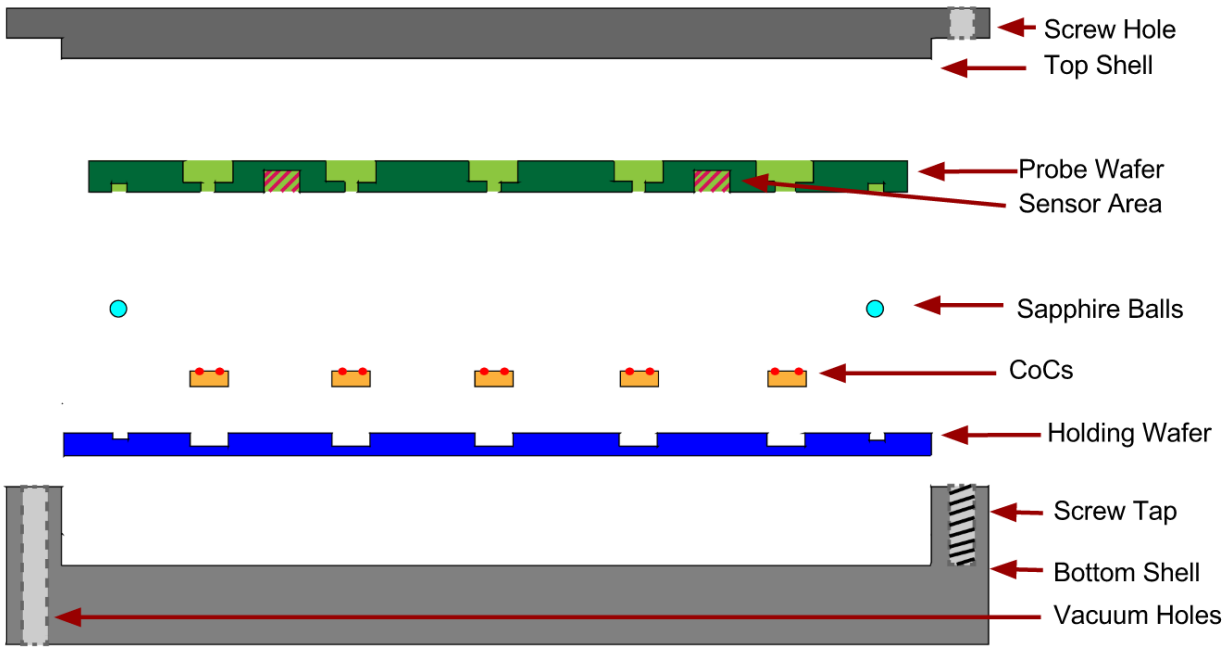



**Figure 2:** Exploded view of the shell assembly

# 2 Assembly

The system developed for Kaiam is an assembly consisting of two silicon wafers, an aluminum shell, cartridge heaters, and an edge connector to power the device and break out signals. The silicon wafers are designed to be placed on top of one another and aligned by a set of sapphire balls. The bottom, or holding, wafer holds the CoCs and breaks out signals to a PCB, while the top, or contact, wafer carries power onto the diodes by using cantilever beams to probe the pads on the CoCs. The aluminum shell houses the silicon wafers to facilitate their handling on the factory floor. The shell also contains cartridge heaters to meet the temperature requirements of the burn-in procedure. The final element of the assembly is the connector system, not pictured in Figure 2 below, that protects against ESD events and communicates with external controllers. Figure 2 shows an exploded view of the primary features of the shell assembly.

## 2.1 Top Wafer

The top wafer will be placed on top of the bottom wafer by the MRSI die bonding machine immediately after CoCs are loaded. Its purpose is to make electrical connections through flexible MEMS probes to the contact pads on the CoCs so that the diodes can be powered by the external controller. The top wafer can move independently of the bottom wafer and the rest of the assembly in order to not have any permanent electrical connections. Therefore, it contains two sets of cantilevers, one of which rests on the CoC pads and one of which rests on conductive pads on the bottom wafer. The electrical connections travel from the power supply to the bottom wafer, pass through probes to the top wafer, and finally pass through another set of probes to reach the CoC. Return current reaches the ground pin of the power

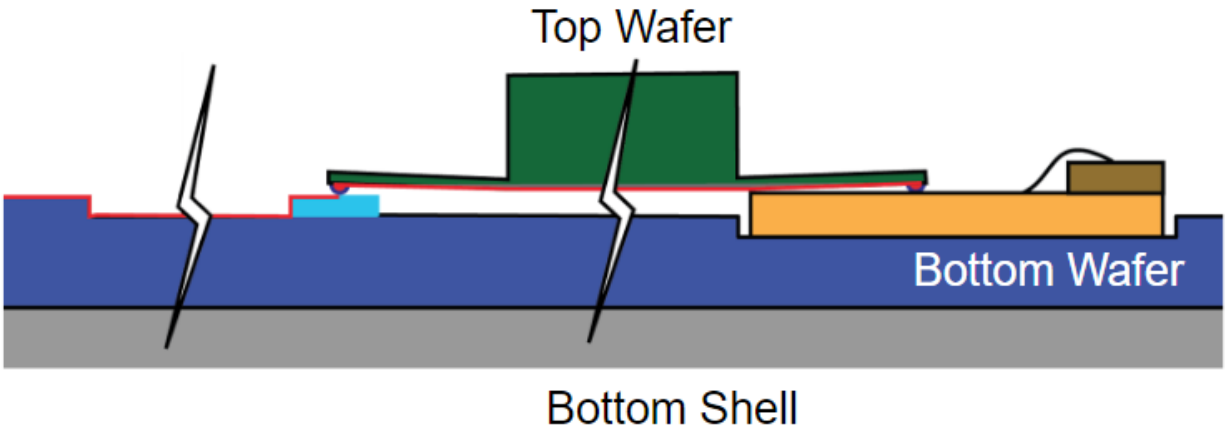



**Figure 3:** Diagram showing the path of current (red) through the power supply (left edge), the top wafer (green), and the CoC (yellow).

supply in the same way. Figure 3 details the signal flow from the bottom wafer onto the diodes.

As shown in Figure 4, the top wafer contains a set of 4 probes for each of the 15 CoCs; each probe makes contact with the individual anode and cathode pads on each CoC. Since each probe's target surface measures under 200 µm in both directions, both wafers must be perfectly aligned relative to each other between the shells. This is accomplished via tightly toleranced sapphire balls, which sit permanently in the bottom wafer and are further discussed in Section 2.2.1.

Gold balls of diameter 100 µm are placed at the tip of each cantilever to ensure that they make contact. These gold balls allow the probes to reach down far enough to contact the CoC pads. The inner probes, which contact metallized areas flush with the surface of the bottom wafer rather than raised pads, have larger contact surfaces designed to accommodate 200 µm diameter gold balls.

### 2.1.1 Stackup

The vertical dimensioning and tolerancing for the entire assembly requires careful consideration. If there is too much space between wafers then the cantilevers will exert little force on the CoCs and make poor electrical contact. If there is too little space between the wafers then the silicon cantilevers will break. The machining tolerance on the top and bottom shells, thermal expansion, gold-ball deformation and CoC height tolerances were accounted for to determine the maximum, nominal and minimum flex that the cantilevers will experience. This accounting is depicted in Figure 5.

As pictured in Figure 5, hard stops are the points where the top shell meets the bottom shell. These points will enforce the ideal space between wafers, and the design of the stops is discussed more in Section 2.4. Each of these hard stops has a vertical tolerance of $-13$ µm based on machining hardware available at HMC. The CoC's vertical tolerance is $\pm 5$ µm based on data measured by Kaiam. Thermal expansion effects decrease the minimum deflection

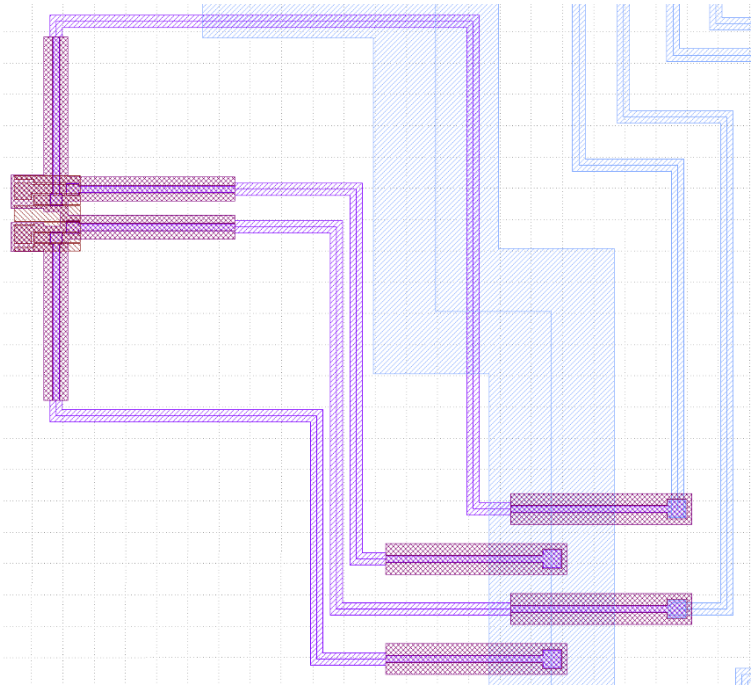


**Figure 4:** Top view of one set of top wafer probes and metallization (purple), and bottom wafer metallization (blue). The thick blue trace on the bottom wafer is the ground pad.

by 1 µm during operation, but maximum deflection will happen at room temperature. Gold ball deformation reduces flex at maximum deflection and is insignificant at the minimum deflection because the force applied to the gold balls is small. The analysis of thermal expansion and gold ball deformation are discussed further in the following section. Therefore, with a minimum deflection of 10 µm, the cantilevers require a nominal deflection of 42 µm and a maximum deflection of 73 µm.

This estimate does not take into account the thickness tolerance of the wafers. If tighter tolerances are needed, the easiest fix is to order the shells with tighter manufacturing tolerance. However, not only is the hard stop height dimension important, but also the flatness of the surface and the parallelism of the top and bottom surfaces.

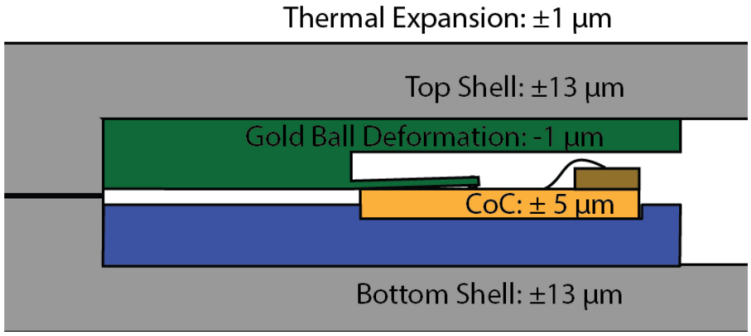



**Figure 5:** Tolerances of all the pieces that affect the deflection of the cantilevers on the top wafer.

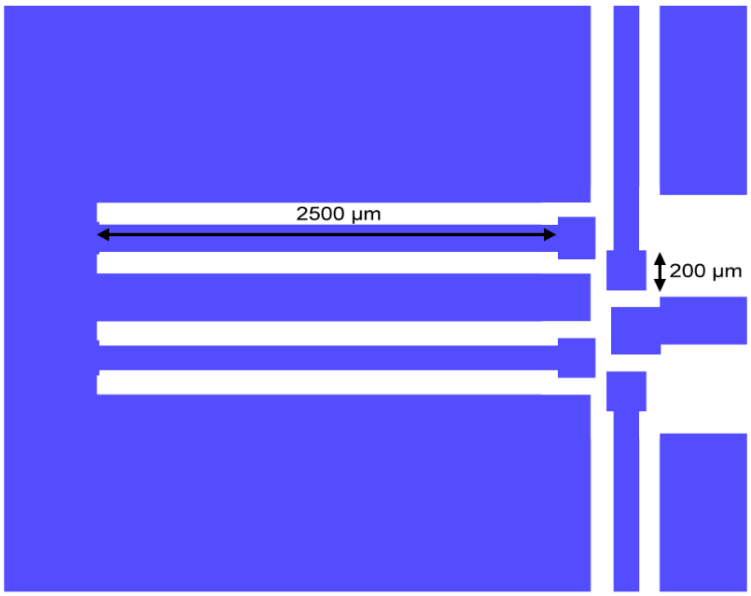



**Figure 6:** Close up of the four cantilevers designed to make contact with the 4 pads on the CoC and hold the CoC in place.

### 2.1.2 Finite Element Analysis

The vertical tolerances from the stack up calculations in the section above were used to guide the design of cantilever dimensions. The minimum allowable cantilever flex to make good electrical contact was chosen to be 10 µm[1]. Therefore, the corresponding maximum flex is 58 µm based on tolerances derived in the stack up.

Figure 6 shows a top down view of the cantilevers with the length, width and height labelled. The height of the cantilever is defined by Kaiam's manufacturing process to be 35 µm. The length was set to 2.5 mm because it was the maximum length before the outer cantilevers crowded the inner cantilevers on the bottom edge.

The cantilevers are paddle shaped to accommodate the gold balls. In order to achieve a gold ball height of 50 µm, a ball of diameter 100 µm or more needs to be deposited at the end of the cantilever. Because of surface tension, the gold can only be deposited on the metallized area so the cantilever width would need to be 20 µm bigger than the largest gold ball diameter. Making the entire cantilever wider than 150 µm would require violating other design rules. Using a paddle instead enables the cantilever to be narrow while allowing for a greater range of gold ball sizes.

Solidworks Finite Element Analysis, or FEA, simulations were used to determine maximum flex possible using these constraints at varying cantilever width from 50 µm to 300 µm. The maximum width while still achieving a safety factor of 2x was 100 µm. This narrow-section width allows for a trace width of 80 µm, which is plenty to deliver the required current over the short distance. Figure 7 shows the stress distribution for these dimensions.

FEA simulations were also used to determine the deformation of the gold balls when the

[1]This number was derived from the equations for contact resistance between two metals. At 10 µm, the voltage drop with 150 mA of current becomes negligible. See page 15 of Spencer, M. E. (2015). *Design Considerations for Nano-Electromechanical Relay Circuits*. University of California at Berkeley.

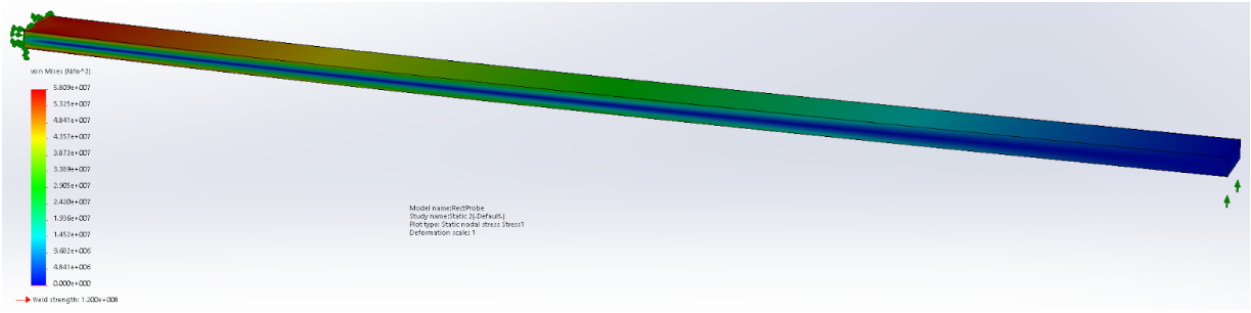


**Figure 7:** Deformation simulation for the narrow section of the cantilever using the dimensions 2.6 mm x 35 µm x 100 µm. The colors show the von Mises stress distribution. The highest stress is $0.8 \times 10^7\,\mathrm{N\,m^{-1}}$ and the yield stress is $1.2 \times 10^8\,\mathrm{N\,m^{-1}}$, more than double the maximum stress at a displacement of 40 µm.

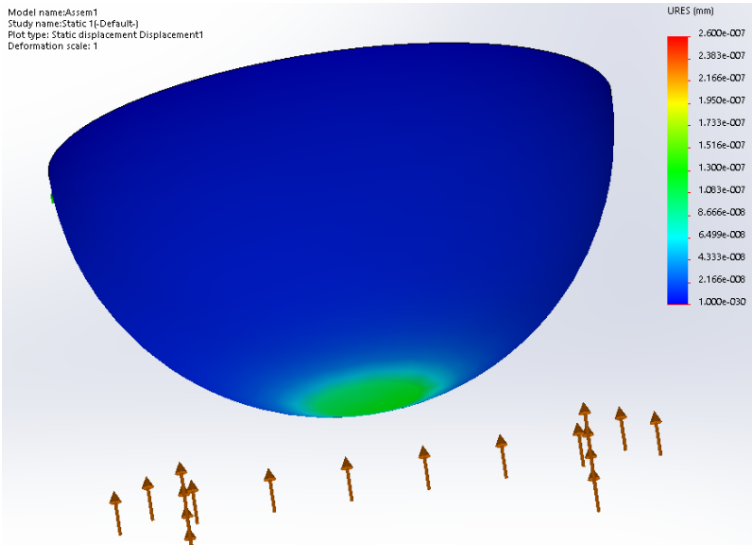



**Figure 8:** Gold ball deformation simulation with constant force applied to the bottom.

cantilevers were flexed and the thermal expansion of the shell and wafers when they was at burn-in temperature. Figure 8 shows an example of the gold ball deformation simulations, and Table 1 shows the results for minimum, nominal and maximum deflection of the cantilevers. The spring constant was derived from Equation 1[2].

$$k = \frac{Ewt^2}{4L^3} \tag{1}$$

This equation assumes that the length is much larger than the width and the deflection is small, which are both true for these cantilevers. The simulation results show that gold ball deflection will be negligible under operating conditions. Additional testing will be necessary to determine if the deformation is purely elastic or if the wafers will need to be re-balled after extended use.

[2]Senturia, S. D. (2001). *Microsystem Design*.

| Cantilever Flex (µm) | Spring Constant ($N\,m^{-1}$) | Force Applied (N) | Gold Ball Deformation (µm) |
|---|---|---|---|
| 10 | 3.66 | $3.66 \times 10^{-5}$ | 0.022 |
| 35 | 3.66 | $1.28 \times 10^{-4}$ | 0.092 |
| 58 | 3.66 | $2.12 \times 10^{-4}$ | 0.17 |

**Table 1:** Gold ball deformation for minimum, nominal and maximum deflection of the cantilevers.

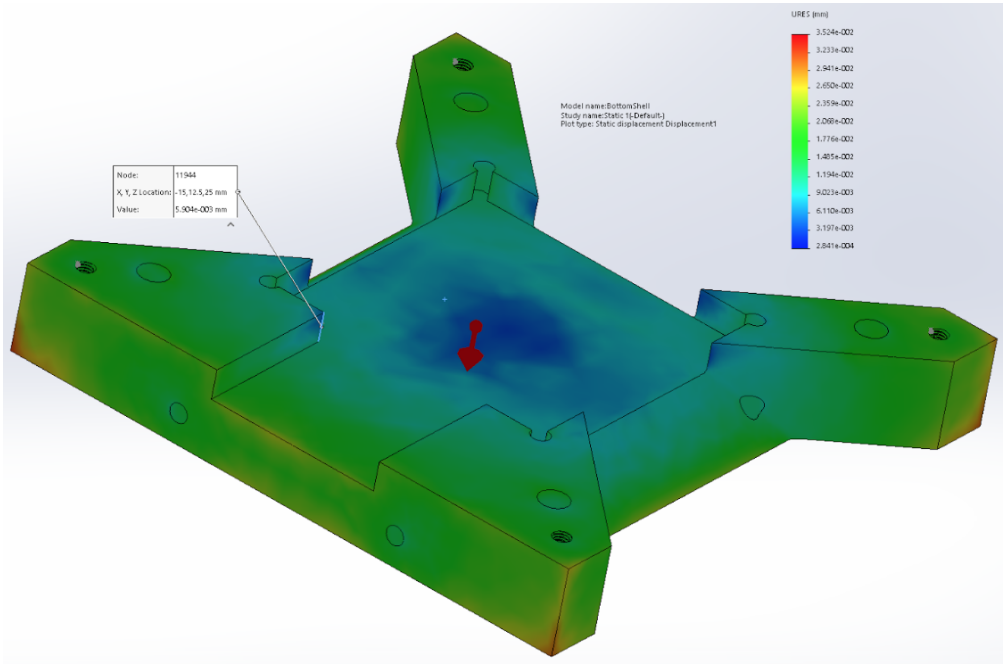



**Figure 9:** Shell thermal expansion simulation done at 150 °C.

Figure 9 shows a simulation of the thermal expansion of the shell during burn-in at 150 °C. The design allows for significant change in the horizontal dimensions of the shell, so the only expansion that matters is in the vertical direction. The horizontal dimension can expand without affecting burn in because the silicon wafers are not glued to the shell and expand separately at the same rate as the CoCs. Also, the horizontal expansion is not significant enough to overcome the flexibility of the wire bonds. The simulation shows a 1 µm increase in the height of the wafer cavity between the top and bottom shell in the worst case. This has already been accounted for in the vertical tolerancing above.

### 2.1.3 Wafer Fabrication Process

The fabrication processes for both top and bottom wafers have several common steps. Both wafers are created using a two-mask process on a nitride-coated wafer, 735 µm thick. The first mask and etch, with Cl plasma, defines the conductive traces on the wafer, while the second mask and etch, at a depth of 80 µm, defines the physical features of the wafers. That is, the CoC and thermistor cavities for the bottom wafer, and the upper cantilever flex

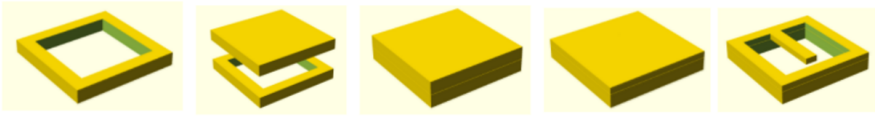


**Figure 10:** Wafer bonding process overview. Thick wafer cavities are shown going through the wafer for visibility.

cavities for the top wafer. For the bottom wafer, a third etch with another set of masks must actually be performed, as the thermistor cavities must be etched deeper than the CoC cavities.

Aside from this last etch, the fabrication steps are common to both wafers. However, the top wafer requires additional fabrication steps for the cantilevers. It is composed of two smaller wafers (known as the "thick wafer" and the "thin wafer") that are glued together using a process known as wafer bonding.

The thick wafer is created using a simple process: an 80 µm etch delineates the outlines of the cavities into which the cantilever probes flex. Once the thick wafer has been etched with the cavity outlines, a second wafer is attached flush with the first one and ground down to a width of 35 µm; this becomes the "thin wafer". Finally, the thin wafer is sputtered, metallized, and etched with the probe outlines. Figure 10 describes a simplified overview of the process of bonding a thick and thin wafer to establish a cantilever and a cavity into which it can flex.

## 2.2 Bottom Wafer

The bottom wafer carries out several important functions. It contains the recesses which hold the CoCs, the recesses which hold sapphire balls that, in turn, hold the top wafer in precise alignment with the CoCs, and the recesses which hold the thermistors used for thermal control. Finally, it routes connections from the top wafer out to the main power supply and the control board.

During the burn-in process, each CoC sits in one of fifteen etched recesses around the perimeter of the bottom wafer, each one of which lies directly underneath four probe cantilevers on the top wafer. The larger, inner cantilevers on the top wafer make contact with an inner metallized layer on the bottom wafer. The metal layer on the bottom wafer routes the anodes of the laser diodes to the control pins and connects the cathodes to a large ground trace.

Four 0402 surface-mount thermistors are set into the bottom wafer; they monitor the temperature of the diodes. These thermistors enable closed-loop control of the wafer temperature. Recesses for these thermistors are etched into the bottom wafer. Pads on either side of each thermistor allow them to be connected to the temperature controller via the same PCIe edge connector as the diodes.

The bottom wafer has 36 metallized pads broken out to its topmost edge. Four correspond to thermistors; two correspond to ground, and the remaining 30 correspond to the diode contacts.

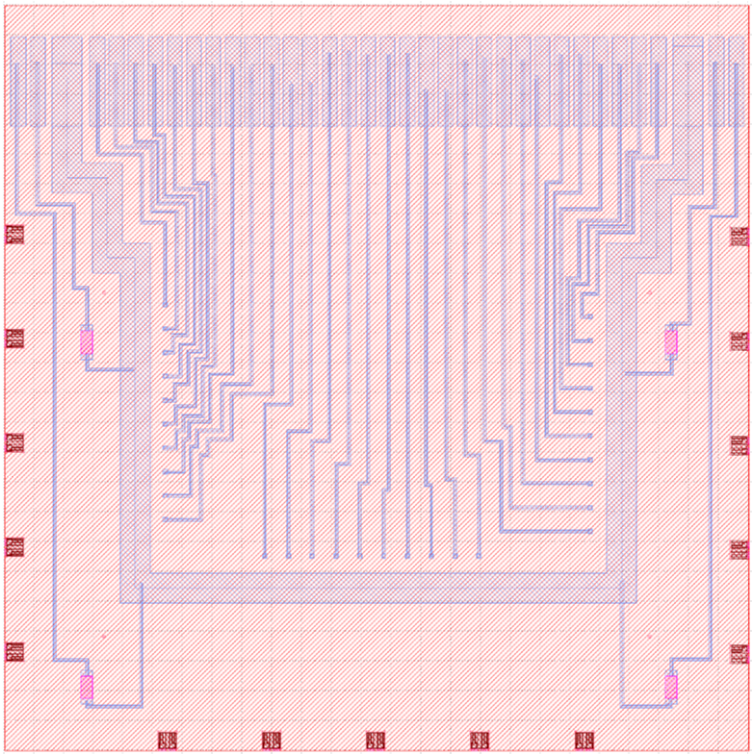


**Figure 11:** Bottom wafer layout. Pink rectangles: Thermistor recesses; pink circles: sapphire ball recesses; thick blue trace: ground ring; thin blue traces: anode and thermistor breakouts; top row of pads: breakout to connector PCB.

### 2.2.1 Sapphire Balls

Four sapphire balls measuring 200 µm in diameter, embedded in the bottom wafer, enforce precise x-y alignment when the top wafer is placed onto it, as shown in Figure 12. Sapphire balls are rigid, available at relatively low cost, and cut to tight tolerances. Four circular recesses, one per sapphire ball, are etched into both wafers. The recesses in the bottom wafer are sized such that the sapphire balls fit snugly but do not make contact with the bottoms of the recesses, while the circular recesses in the top wafer have a slightly larger diameter than the sapphire balls. Thus, the top wafer recesses will fit completely around the sapphire balls. These holes allow gravity to guide the top and bottom wafers together in alignment as pictured in Figure 12.

### 2.2.2 Process Router

The fabrication process for the bottom wafer is very similar to that of the top wafer, up to the wafer bonding step. The bottom wafer does not require wafer bonding because it does not have any cantilevers. The wafer is processed through a two mask process that defines metallization with a gold etch and recesses for CoCs, sapphire balls and thermistors with DRIE. An additional 80 µm etch is applied to the thermistor recesses to ensure that the thermistors sit deeply enough in their recesses to not interfere with the top wafer. This additional thermistor etch requires particularly thick resist to coat the 80 µm sapphire ball

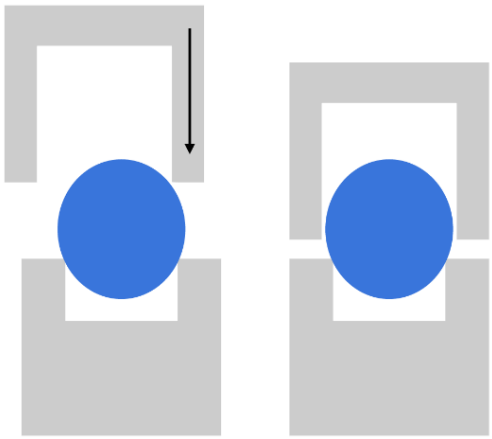


**Figure 12:** Sapphire balls align corresponding recesses in top and bottom wafers.

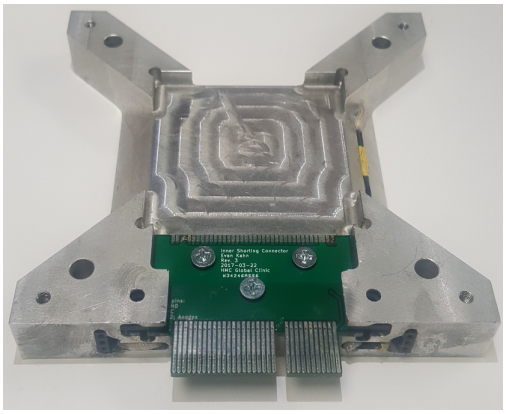


**Figure 13:** Shorting connector board mounted to the shell that breaks out the connections from the wafer to a 64 pin male edge-card connector. The pads along the top get permanently wire bonded to the bottom wafer.

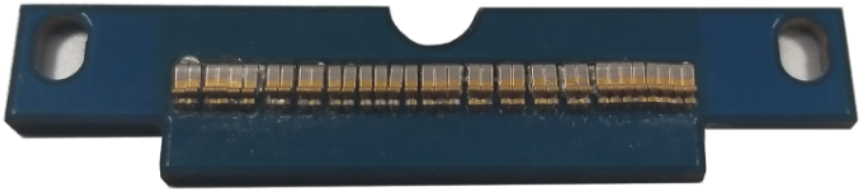
and CoC recesses.

## 2.3 External Connectivity

In order to power the diodes, a PCB breaks out the connections from the wafer to an external 64-pin PCIe edge card connector as shown in Figure 13.

One particular challenge with this edge card connector is the need for electro-static discharge, or ESD, protection. Commercial ESD protection solutions typically rely on parallel capacitors, relays or diodes which redirect current away from the devices under test. However, the laser anodes and cathodes must be shorted directly to the edge connector and must be protected against shorting even when the assembly does not receive power, which means that ESD-safe operation could not be guaranteed with standard solutions such as these. A custom "shorting connector" was designed to prevent ESD events through the diodes. It shorts all the laser anodes to each other when the assembly is disconnected from its power supply.


**(a)** Connector with shroud



**(b)** Shroud PCB

**(c)** Shorting connector side view

**Figure 14:** (a) The shell with both the shorting connector PCB and the shroud PCB mounted. (b) Shorting connector shroud with "teeth." (c) Side view of the shorting connector showing the plungers holding the shroud in the shorted position.

### 2.3.1 Shorting Connector

The shorting connector board consists of 36 pads that will be connected directly to the wafer, which are routed to one side of a standard male PCIe edge card connector. Another board, the "shroud", sits directly over the connector and contains of an array of metal teeth that make contact with the connector as pictured in Figure 14. The shroud PCB has "teeth" on its underside which are designed to short together the 32 top pins on the green PCIe edge card connector. When the PCIe edge card mates with its socket, the blue PCB is pushed forward against two springs and the "teeth" slide off the tops of the PCIe pins. The 36 exposed pads for diode and thermistor connection at the top of the shorting connector PCB correspond directly to the row of 36 exposed metal pads along the topmost edge of the bottom wafer. Since both the shorting connector PCB and the bottom wafer will be permanently installed in the bottom shell, they can be permanently wire bonded together.

Since the diodes should be shorted to ground when the shroud is active, the first two pins

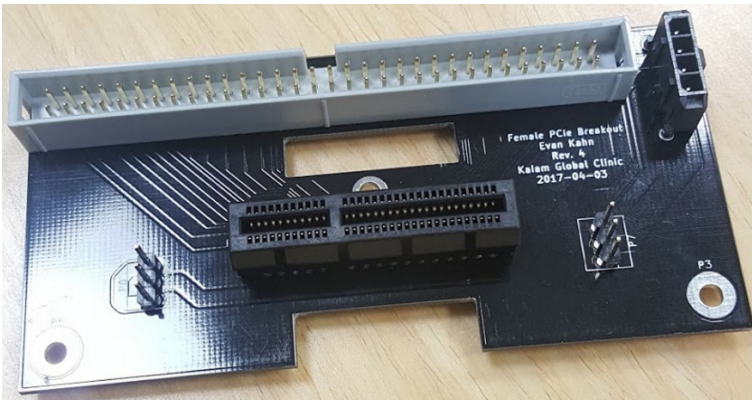



**Figure 15:** The female PCIe breakout PCB with the PCIe connector and power connectors for the shell on the bottom. The connectors on top go to the control PCB.

on the male PCIe connector are ground. Pins 3-32 on the top of the male PCIe connector are the diode signals. On the bottom of the connector, the four pins closest to either edge are the thermistor signals and the rest are ground.

### 2.3.2 Female PCIe connector PCB

The PCB in Figure 15 routes the signals from the PCIe shell connector to a 64-pin ribbon cable. It also provides power to the heaters embedded in the shell. The power connection is made using header pins. The board also contains a slot for a right angle bracket to mount the shell into the enclosure (see Section 3). The board has three screw holes; the middle one holds a nylon screw to prevent flexure of the board during operation.

The power connectors for the cartridge heaters must withstand the high temperatures encountered during burn-in. MIL-spec connectors rated for high temperatures usually feature latches that would prevent technicians from safely removing the assemblies from the enclosure. Header pins capable of withstanding 150 °C were used to make the power pins instead of standard MIL-spec connectors. These allow the assemblies to be safely inserted and removed from the enclosure.

## 2.4 Shell

The shell is the aluminum structure which protects and holds the silicon wafers. It is comprised of two halves, a top and a bottom, which are pictured in Figure 16. The two silicon wafers rest against the flat surfaces at the center of the shell, and they come into contact at this plane which is precisely dimensioned to control the separation of the wafers and, as a result, the contact force between them. These machining tolerances are discussed in Section 2.1.1.

This surface must be as planar as possible to prevent any distortions from damaging the probes or making poor contact. MIC6 cast aluminum enables easier machining of this piece. The tight tolerancing on the primary plane guarantees a particular amount of flexure on the cantilever beams in the top silicon wafer, as described in section 2.1.2. This spacing guarantees stable contact between the electrical pads on the CoCs and the wafer probes which

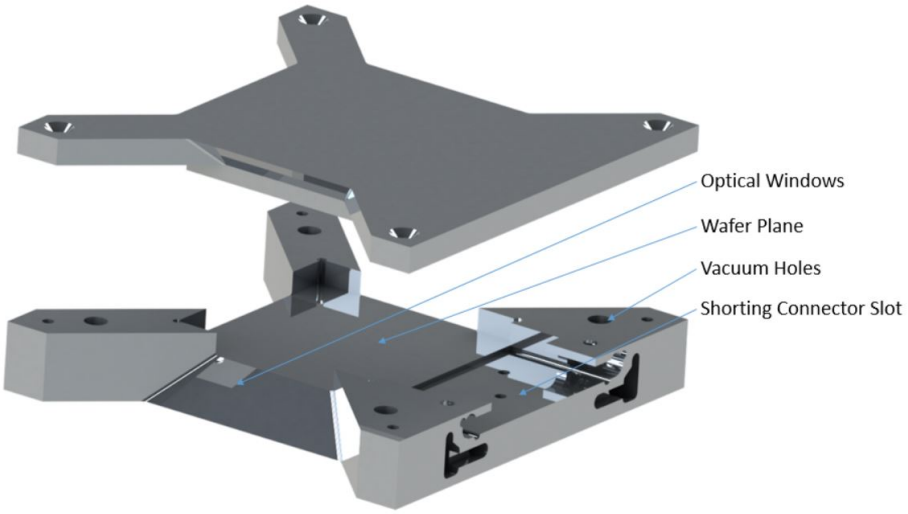



**Figure 16:** Solidworks render of the two shells.

**Figure 17:** The back side of the shell with the connector slots.

is imperative for successful burn-in testing. Additionally, the spacing prevents a technician from holding the shell too tightly and damaging the probes.

The outermost through-holes on the bottom shell allow the MRSI die-bonder's vacuum to secure the assembly together as thumbscrews are added through the tapped holes of the top shell. The MRSI die-bonder can apply this vacuum and add the thumb screws, so there is no need for an technician to handle the shell until it is fully assembled. Once it is assembled, technicians can handle the shell without damaging the wafers because forces applied to the shell will be applied to the hard stops.

The shell is cross-like with 45° chamfers on the three sides with exposed diodes, as shown in Figure 16. The conical output from the laser diodes is visible through the chamfered windows without being blocked by the structure of the shell. This allows for the laser output power to be measured without removing CoCs from the shell. Additionally, slots for cartridge heaters were positioned below the diodes on the silicon wafers to ensure even heating of the laser diodes.

The edge connector, shorting PCB, and two of the cartridge heater headers lie on the windowless side of the bottom shell. The bottom shell, shown in Figure 17, has tapped holes so the edge card connector can be affixed to the shell. The shell has a channel which guides the shorting PCB as it slides onto and off of the edge connector pins. A spring embedded in the shell controls its maximum displacement.

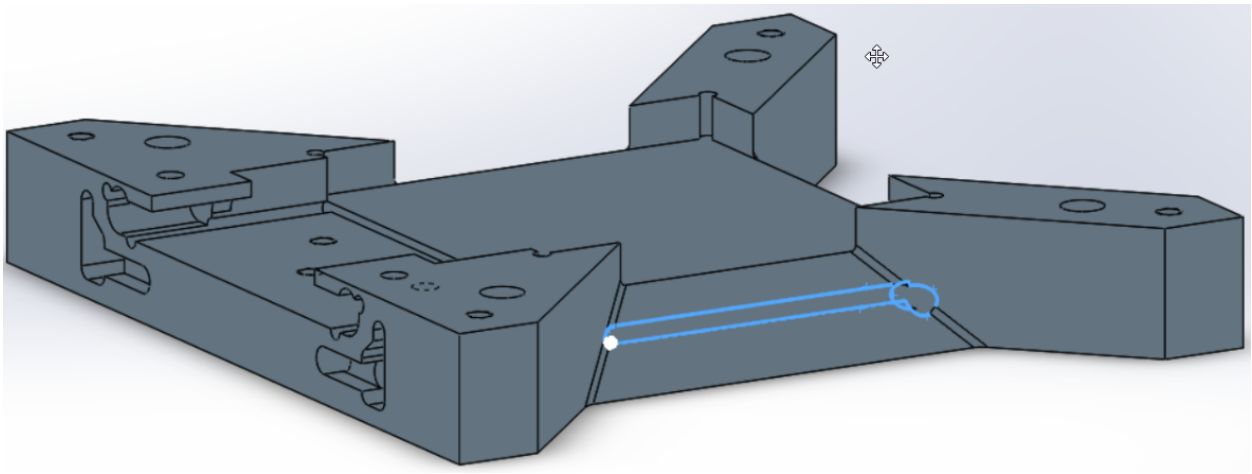


**Figure 18:** The shell's channel on the side for keeping the cartridge heater wires out of the optical chamfer.

To facilitate providing power to the cartridge heaters in the shell, channels were milled in the shell in order to guide the cables directly from the slots to the power connectors, as shown in Figure 18. They are designed to avoid obstructing the radiation from the laser diodes. Putting the channels in the sides also minimizes the distortion of the plane of the silicon wafers. The two channels milled on the back side of the shell provide power to the cartridge heaters in the back, and consist of a small milled hole within a larger milled slot that is slanted such that the power cables that feed the cartridge heaters can easily bend and be attached to the header pins.

Ensuring that the cartridge heaters can precisely maintain the diode operating temperature requires careful simulation to validate the designs. Solidworks Flow thermal simulations were run to investigate the distribution of heat throughout the assembly and ensure that the CoCs will reach 150 °C. The flow simulation consisted of a large contained environment with airflow from top to bottom of $3.4\,\mathrm{m\,s^{-1}}$. The heating elements were three cartridge heaters placed in their designated slots. The cartridge heaters were controlled by a simulated PI control loop. The simulations show that the cartridge heaters require 34 W of power to hold the CoCs at 150 °C.

Kaiam requires that the CoCs stay within ±3 °C. Figure 19 shows a maximum differential of 2 °C (±1 °C) across all the CoCs at steady state. The simulations do not take into account the bang-bang control loop since the program can not handle that type of control. The thermal loop parameters in the controller will also determine the range that the bang-bang control loop will allow the CoCs to reach. However, the design itself is able to heat the CoCs evenly and fits the specified parameters.

A set of 12 V/30 W cartridge heaters were chosen for this design (see Appendix BOM). They were selected to minimize the voltage required and have a maximum operating condition of 24 V/100 W. During testing, the simulations were shown to be overly conservative and 12 V was chosen as the operating temperature. Testing showed that a single shell took around 12 minutes to heat to 150 °C from room temperature with 3 heaters. Test results are detailed in Section 4.2.

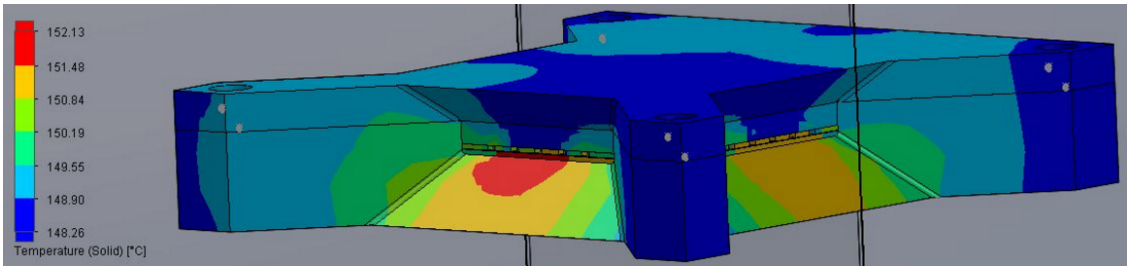



**Figure 19:** Thermal simulation of shell with CoCs and cartridge heaters. The diodes in the middle have a temperature gradient less than two degrees as desired.

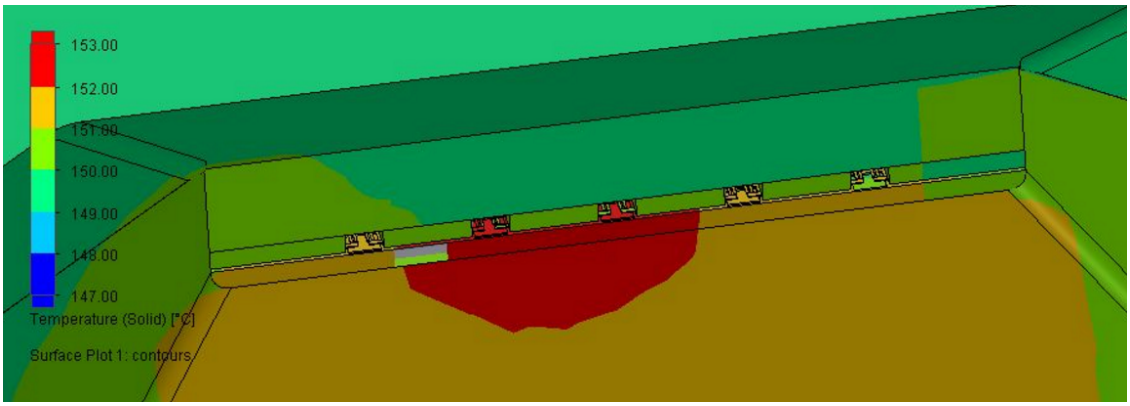



**Figure 20:** Thermal simulation of the shell with CoCs and cartridge heaters with two CoCs not producing heat and three self-heating. The temperature gradient between the 5 diodes still remains within 2°.

One possible concern for the system as it stands is diode self-heating. Since the CoCs are running for the entire burn-in process, they will be producing substantial heat. If some, but not all, diodes fail open and don't self-heat, the gradient across the CoCs will be greater than the $\pm 3\,^{\circ}\mathrm{C}$ allowed. Another set of SolidWorks Flow Simulations, shown in Figure 20, was run to check if this would be a problem. A different number of CoCs were turned off on each side of the shell, and the overall gradient was still found to be $\pm 1\,^{\circ}\mathrm{C}$ as before. Therefore, the diode self-heating should not impact the overall accuracy of the temperature control system.

## 2.5 MRSI Assembly

Prior to placing the elements of the assembly into the MRSI machine, the bottom wafer and the bottom shell need to be bonded together. The bottom wafer must be wire bonded to the inner pads of the male PCB connector on the bottom shell. Then the sapphire balls must also be permanently fixed into the recesses in the bottom wafer. Next, a gel pack containing CoCs to undergo burn-in must be manually placed into the MRSI die-bonder, and the top wafer must be placed into a special chuck in the MRSI to hold it without breaking the MEMS cantilevers when facing down. Finally, the top shell and screws required for fastening the assembly must be placed in the MRSI.

The assembly process itself begins by taking the permanently bonded bottom shell and wafer and placing them into the MRSI machine. Then, the machine should pick up each CoC from its respective gel pack and load them into the bottom wafer. The CoCs should be facing outwards such that the diode laser output can be measured from outside the assembly. Next, the die-bonder should pick up the top wafer and place it on top of the bottom wafer in alignment according to the location of the sapphire balls, as well as CoC pads. The top shell should then be placed on top of the assembly. At this point, the MRSI machine should pull a vacuum through the holes on the bottom shell in order to compress the assembly together to its final position. Finally, the MRSI machine should screw the four corner screws into place such that the assembly remains compressed and ready to be picked up by a technician.

# 3 Enclosure

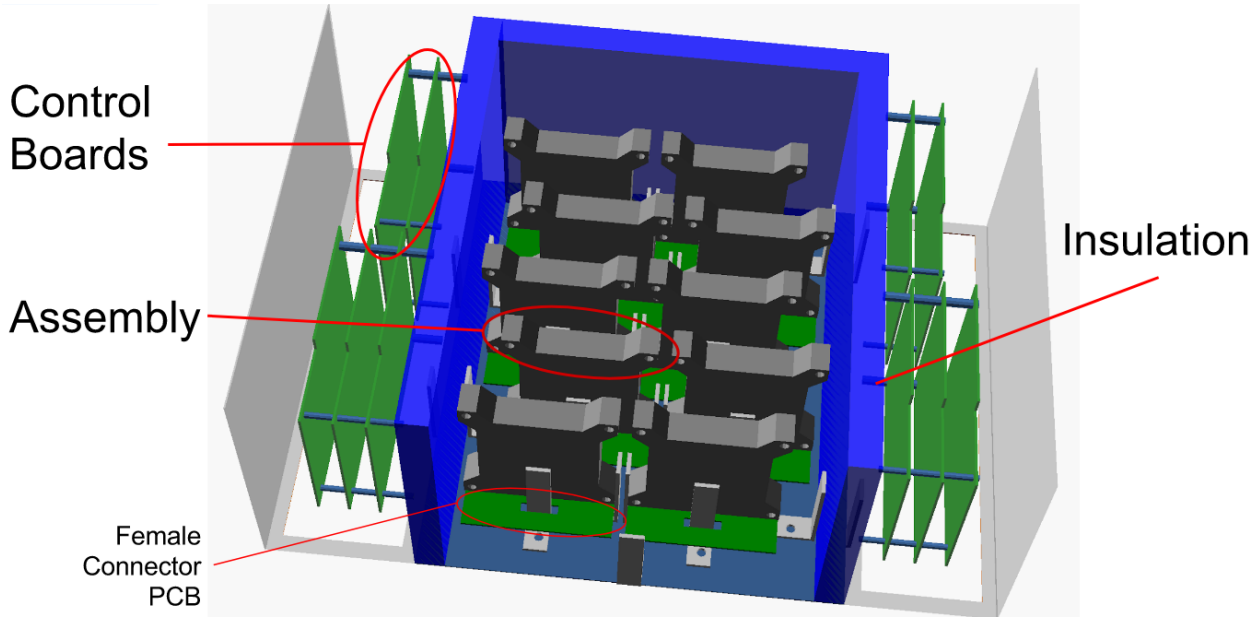
The enclosure consists of a 19 in server rack and a set of standard 4U drawers. Each enclosure drawer houses shell assemblies, which are described in Section 2, and driver boards, which are described in Section 4. The drawers are designed to organize these assemblies in a space-efficient manner and maintain the driver boards at a safe temperature. The assemblies are staggered in two rows within the central compartment of the drawer. Female PCIe connector boards (see Section 2.3.2) and right-angle brackets are bolted to the bottom of the drawer. The brackets guide the placement of the shell assembly into its dock on the female connector board and provide mechanical support. The driver boards are placed in a separate compartment on the sides of the drawer. This compartment is open to ventilation so the boards can be cooled. They are held in place by metal spacers and nuts mounted through holes on the sides of the drawer. Blocks of ceramic fiber insulation isolate the assemblies from the driver boards,which helps to control the temperature of the driver boards. An additional block of insulation placed against the front wall of the drawer keeps its handle cool. The insulation blocks are sealed with sheet gasket material to prevent loose particles from contaminating the clean room environment of the Kaiam factory floor. A CAD mockup of the internal layout of a drawer is shown in Figure 21, followed by an image of the constructed physical prototype.

Figure 22 shows the placement of the right-angle brackets and female connector boards on the floor of the drawer. A dimensioned drawing of the holes needed for mounting them is in Appendix A.

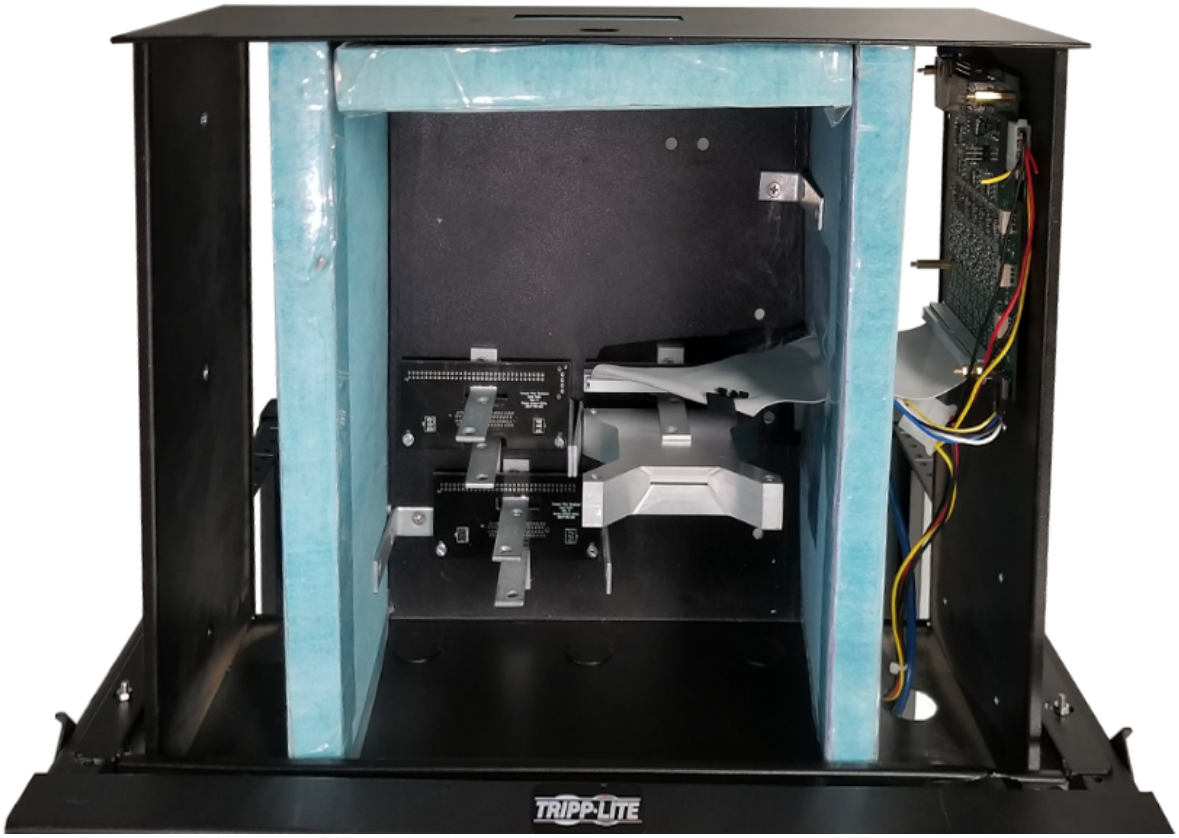
## 3.1 Thermal

A thermal simulation using SolidWorks Flow Sim was conducted on a stack of eight drawers in an environment box with flow conditions of $3.6\,\mathrm{m\,s^{-1}}$ air flowing in through the top and out through the bottom. The holes cut away above and below the driver board compartments on the sides allow for unobstructed airflow past the driver boards and through multiple drawers. They can be seen on the top surface of the drawer CAD in Figure 23 below.

The goal of the design was to maintain the temperature of the driver boards below 60 °C and the simulation produced satisfactory results. A plot with the simulation results for the full stack of enclosures is shown in Figure 24.

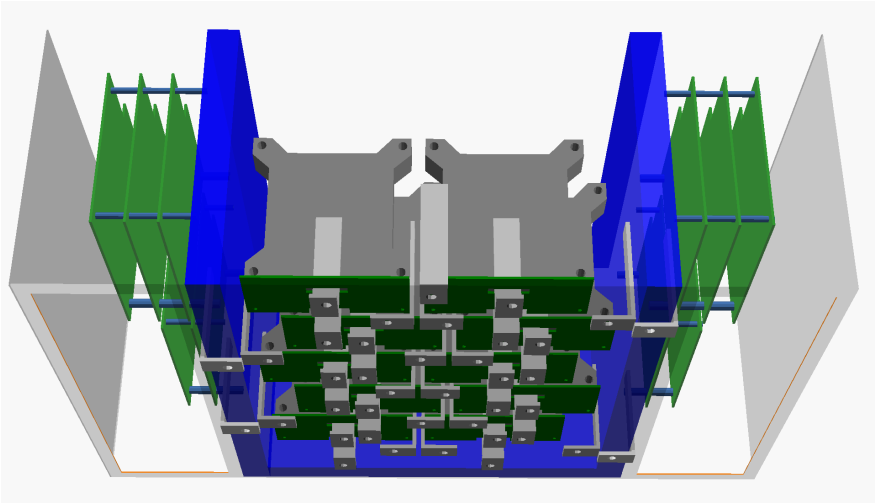



**(a)** Complete enclosure CAD

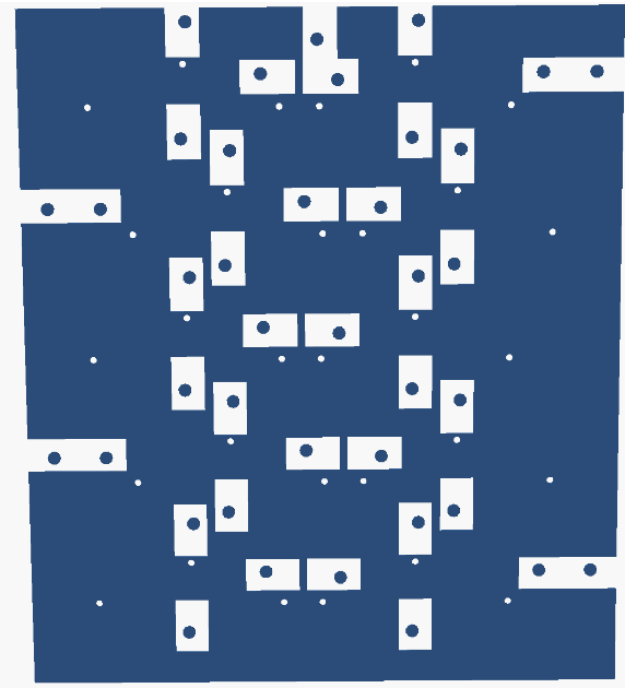



**(b)** Drawer prototype

**Figure 21:** (a) Image of Drawer CAD viewing from the back and top. (b) Image of enclosure drawer prototype with similar view as CAD image above.



**(a)** 3D view



**(b)** Bracket and PCB mounting positions

**Figure 22:** (a)Image of Drawer CAD viewing from the back and top. (b) Bottom surface of drawer from the same bottom view as the image above, showing holes for right-angle brackets and female connector PCBs with footprints of right-angle brackets.

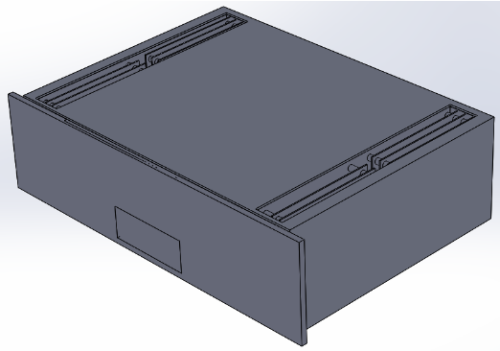


**Figure 23:** SolidWorks Drawer CAD showing top holes cut away.

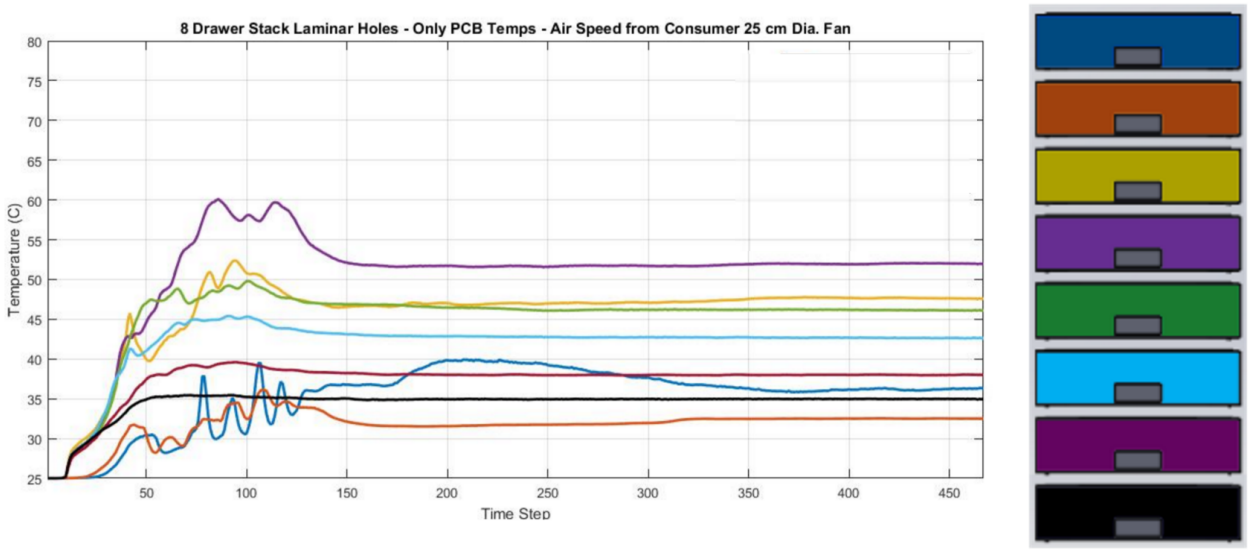



**Figure 24:** Plot of thermal sim results for driver boards in each drawer for a stack of eight.

Cooling fans were used to generate the required volumetric flow rate past the driver boards at the correct air velocity based on the $3.6\,\mathrm{m\,s^{-1}}$ air velocity from simulation. Equation 2 was used to determine a conservative estimate of the fan parameters needed to generate this flow. $Q$ is volumetric flow rate in CFM, $v$ is the air velocity and $A$ is the cross-sectional area of the sections containing the driver boards.

$$Q = vA \tag{2}$$

The results suggested that six 4.5 in fans rated at 100 CFM would suffice. However, 250 CFM fans were chosen instead to allow significant margin in cooling. These fans are fixed onto the top of the rack such that the airflow runs directly through the holes in the drawers for the driver boards. Figure 25 below shows the physical prototype fan mount with a fan controller (refer Appendix B) on the rack.

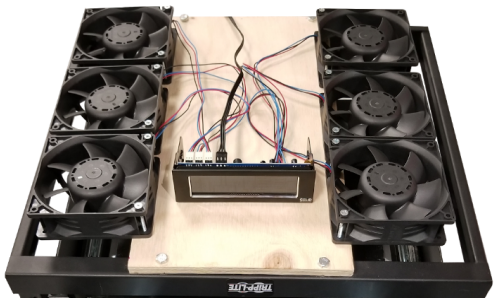


**Figure 25:** Fans mounted to the top of the rack directly above the holes cut for control PCB cooling. The central control unit uses closed loop control to maintain the control PCBs at a safe temperature.

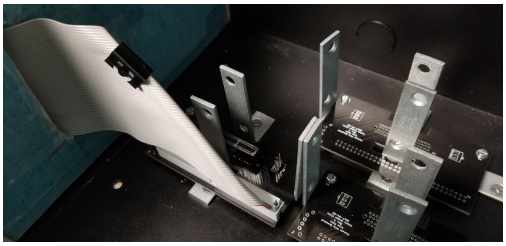


**Figure 26:** Ribbon cable routing example. After each cable is folded and folded as shown, their routed directly to the insulation and then run along the insulation until they reach the through hole shown on the left.

## 3.2 Wire Managment

There are many wired connections to and within the enclosure. Inside the drawer, 10 64-pin ribbon cables connect the driver boards and the shell assemblies. The ribbon cables run through a slit in the insulation blocks to make these connections between enclosure compartments. These slits are sealed to avoid particle emissions from the ceramic fiber insulation. In the section of the drawer with the assemblies, the ribbon cables can be organized and protected from the hot shells by folding them and holding the fold in place with clips as shown in Figure 26.

There are also Ethernet and power cables running through the back of the drawer for each of the driver boards. The cables will need to touch the hot back of the enclosure as they leave the drawer. Heat resistance wires[3] were chosen instead of a heat resistant exit port because the cables will need slack in them when the drawers are closed. This extra slack will likely touch the backs of hot drawers below.

[3]The price estimate in Appendix B includes a quote for these Ethernet cables. http://www.tpcwire.com/products/wire-and-cable/bus-cables/ethernet-cables/chem-gard-200-c-cat6-industrial-ethernet-cable

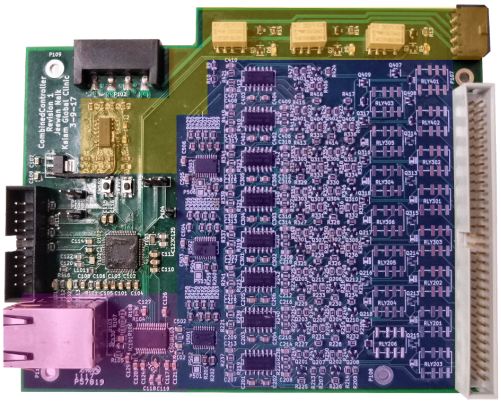


**Figure 27:** Control board with the networking circuitry highlighted in pink, the current control circuits highlighted in blue, and the temperature control circuit highlighted in orange.

# 4 Control

The current and temperature of the diodes are controlled by a driver board. One driver board is capable of controlling one assembly, so there are equal numbers of assemblies and driver boards. Each board contains a single SAM4S microcontroller which communicates with a central computer through an ethernet controller, sets the setpoint for all of the current control loops and runs the bang-bang control loop to control the temperature of the assembly. Each of these circuits is highlighted in Figure 27 and are described in more detail in the following sections.

## 4.1 Network & UI

A full rack, containing eight drawers, needs to allow 80 boards to communicate with a single computer. To facilitate this, each board contains an ENC28J60 ethernet controller. This chip was chosen because it is popular, has a well-made datasheet, and communicates with the SAM4S microcontroller through SPI, an easy to use interface. A single computer on the factory floor can be plugged into any number of racks as long as each board has a unique MAC and IP address, which is achievable with the ENC28J60 chip. Figure 28 shows a map of how information is sent between pieces of the network.

The single computer, connected to the boards through an Ethernet switch, runs a GUI developed on top of a Python library supporting core burn-in functionality. The Python library is extensible, compartmentalizing each individual shell that must be controlled into its own object. By default, the Python library will instantiate a preset number of Shell objects, organized into a number of Drawer objects; each Shell will be linked to a unique MAC address, which can be loaded from a text file. If there is no MAC address corresponding to a certain location in the burn-in rack, it can be specified by the user. Once a MAC address is assigned to each Shell object, the control computer verifies that bidirectional contact is possible by sending a packet with initialization information.

Since there is no guarantee that a control board will always be used with a specific shell and thus a specific set of thermistors, the program also provides functionality to assign thermistor calibration coefficients to each Shell object. This process must be re-run each

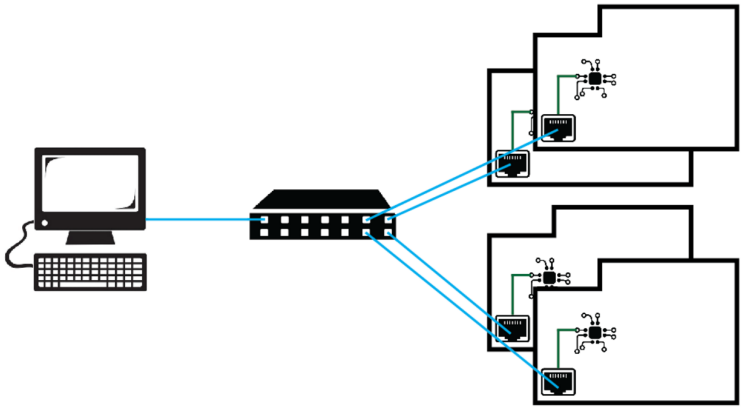


**Figure 28:** In order to interface with the user, the boards are connected via a switch to a central computer with a GUI for technitians.

time the physical shells are placed in the drawers. Ideally, the aluminum shelves themselves will be permanently engraved with a four-digit code, which will allow the Python framework to search for its corresponding set of thermistor calibration coefficients and send them to the temperature control board on startup.

Once each board in the rack has an assigned MAC address and set of temperature coefficients, the temperature and current set point of each Shell object can be both specified and monitored by the Python library. Ultimately, the Python library is responsible for sending one of five of the following commands to the current control board (some with a data payload):

1. Request information
2. Send temperature calibration data
3. Set shell temperature set point
4. Set shell current set point
5. Disable shell (turn off heaters and diodes)
6. Enable shell (turn on heaters and diodes)

When any of these commands is transmitted via Ethernet to the control board, the board should send back an acknowledgement that the message has been received. Ultimately, a GUI will be built to leverage the Python library. It will streamline the process of associating MAC addresses with each slot in the rack, designating temperature and current set points for each shell, monitoring shell temperature and alerting technicians in the case of component failure, and running for a specified amount of time.

## 4.2 Thermal

The temperature control section of the driver board maintains the temperature of the CoCs at 150 °C. It accomplishes this with a thermal control loop comprised of on-wafer thermistors,

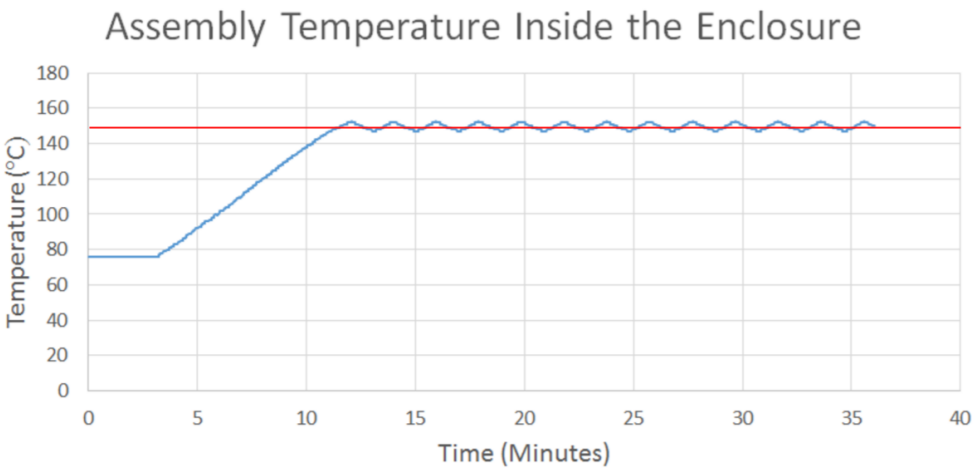



**Figure 29:** Results from the temperature test of a single shell with 3 cartridge heaters inside of the enclosure. A thermistor was mounted to a piece of silicon and placed inside the shell to simulate the actual wafers. The wafer reached temperature after 12 minutes and switched every 90 seconds after that.

in-shell cartridge heaters, on-board relays, and the SAM4S microcontroller. The loop uses a simple bang-bang control law with the upper and lower bounds of the controller set to 153 °C and 147 °C. This control law can be implemented by using relays to turn the heaters on and off.

The thermistors are read by the internal 12 bit ADC on the microcontroller after a voltage is generated through a voltage divider and then passed through a unity gain buffer. The thermistor resistance will go from 10 kΩ to 360 Ω as the temperature increases from room temperature to 150 °C during burn in. The other resistor in the voltage divider is 1 kΩ to maximize the accuracy at high temperatures while still keeping the voltage at the minimum burn in temperature, 85 °C, below 3.3 V. 3.3 V is the maximum voltage that the internal ADC can measure, so the op-amp should be powered from 0 to 3.3 V to stop any voltages above or below that from passing through to the ADC Although the current schematic has the op-amp powered by 5 V, the provided board has the op-amp sky-wired to 3.3 V.

There are 4 thermistors reading the temperature of the four corners of the board and each of the 3 cartridge heaters along the edges can be individually powered. The thermistors are on the corners of the wafer and the cartridge heaters on along the three sides with CoCs, so the temperature used in the bang bang control for each heater is the average of the two thermistors on either side of it.

Figure 29 shows the results of testing the bang bang controller. The results show that the assembly reaches 150 °C in 12 minutes and the relays switch every 90 seconds on the edges of the bang bang control loop. This result is extremely conservative, because the testing was only done on a single assembly in a single drawer. In real life, a drawer has 10 assemblies and the insulation will do a better job of keeping the hot air in,. Also, the insulation will keep the air around 150 °C, so the relays will have to switch much less than in room temperature air.

The lifetime of the board is likely to be limited by the frequency of the relay switching.

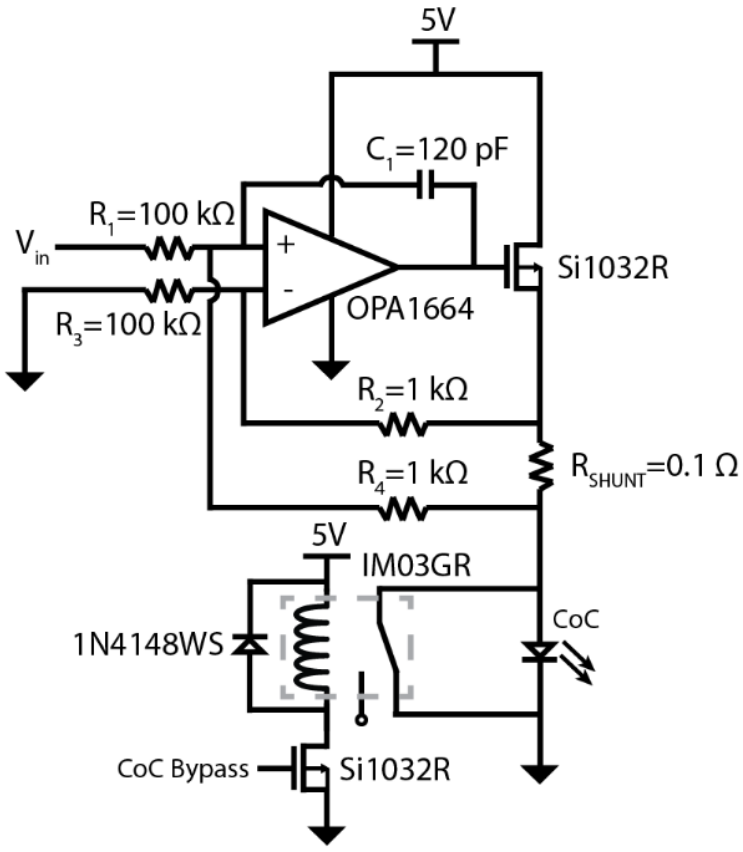



**Figure 30:** Current control circuit which sets the current through the shunt resistor, and therefore the CoC, based on Vin.

The relays have a minimum cycle life of 500,000 operations. Currently, the upper and lower bounds are set to be $\pm 3\,^{\circ}\mathrm{C}$ around the setpoint in order to maximize the time between switching. The switching period of the relays can be further increased by implementing a moving average to smooth out the input signals and reduce the effect of quantization noise. The relays switch on every peak and trough in the graph, or roughly every 90 seconds. Even with this conservative estimate, 90 seconds between switches turns into a minimum board lifetime of 12,500 burn-in hours, or 2 years of 24/7 burn-in.

## 4.3 Current

The current control section of the driver board uses 30 individual analog circuits, shown in Figure 30, to control the current going through each diode in an assembly. Figure 30, along with Appendix B, also contains the part numbers used on the final board.

The current through a diode is controlled by an op-amp which measures the voltage across the a $0.1\,\Omega$ sense resistor and then changes the gate voltage of the MOSFET to match the voltage drop to the setpoint. Equation 3 relates the setpoint to the output current, with the DC offset coming from the voltage divider on the inverting input. This voltage divider is there so when the setpoint is zero and the relay is shorting the anode to the cathode, the

non-idealities of the op-amp do not drive the output all the way to maximum current.

$$\frac{V_{in}}{I_{out}} = \frac{R_3}{R_4} R_{shunt} \text{ and } R_1 = R_3, R_2 = R_4 \tag{3}$$

The setpoint voltages are sent from the SAM4S microcontroller to the DACs via bit-banged SPI. During initial programming of the boards, calibration coefficients are hard coded into the microcontroller for each of the 30 control loops to account for the true resistances of the five current sensing resistors and offsets of board components.

On the user end, the technician simply needs to input the desired current for all of the diodes, and the Python library will send the information to the microcontroller through the Ethernet controller. After the desired current is inputed, the microcontroller waits for the technician to press start and then switches the relay that was holding the anode and cathode shorted together. The anode and cathode are shorted to protect from ESD events while the assembly is plugged into the enclosure (and the shorting connectoxr is de-shorted). After the relay is switched, the microcontroller slowly ramps up the current through the diode over a 1 minute period. This is done to replicate the performance of similar burn-in systems sold by other companies. There is also a ramp-down at the end, and if the current needs to change in the middle, the microcontroller ramps slowly between setpoints. In practice, the inclusion of the relay brings the op-amp input to its rails, causing it to output 5 V and pass too much current through the transistors. To solve this, the next revision of the PCB should include a resistor in series with the relay input to increase the voltage with any current.

Right now the current control circuit can drive at most 120 mA into each diode. This is limited by the transistor on the output of the op-amp, so the limit can be easily increased by selecting a different transistor. The DAC, which controls the setpoint, has 8 bits of resolution, so each step corresponds to 1.3 mA when 1 V represents 100 mA. With proper calibration, there will be a quantized DAC output current will be set within 0.65 mA of the desired burn-in current, which is well within the $\pm 5$ mA goal set by Kaiam. Each DAC comes with 12 programmable channels, ten of which are used by the board. The extra two channels are routed to pads for easy repair if a channel fails.

Two other minor changes for future revisions are the Ethernet connector orientation and the order of pins on the power connector. Right now, the Ethernet connector forces the cord to bend awkwardly against the side of the drawer. By putting the ethernet controller next to the power connector, plugging and unplugging boards would be much easier. Also, the power connector is a common connector found on most power supplies. However, the 5V pin and one of the ground pins in the 4 pin connector are flipped from the standard.

# 5 Future Improvements and Testing

All the goals initially set in the fall have been accomplished to some degree, but work remains before this burn-in solution can be put into production. The wafers manufactured by Kaiam will need to be integrated into the rest of the assembly and tested. Before testing, an MRSI must first assemble these wafers. The assembly testing plan is described in Section 2.5 and needs to be done on site by Kaiam. During assembly testing, this plan can be modified in order to minimize the time on the MRSI both before and after burn-in. These tests will

also verify that the MRSI can consistently pick up the relatively heavy top shell and apply sufficient vacuum to bring the top and bottom shells together before securing them with screws.

In addition to testing with the MRSI machine, the enclosure and UI will be tested for ease of use. Hopefully, the shell can also be tested with a light collector to make sure the entire output of the laser can be received.

A few minor design changes can also improve the performance of the burn-in solution. For example, the relays used in the temperature side of the controller could be replaced with power FETs which can reduce the cost of the board while increasing the lifetime of the board and enabling the use of a PID control loop or tighter bang-bang control. Additionally, the entire prototype is close to fitting into a 3U drawer instead of the current 4U drawer. Changing this would require shortening the legs of the shell or building the female PCIe connector into the drawer. Also, the control board would need to be slightly thinner. The best way to accomplish this would be to change the current control circuits to power multiple diodes in series to reduce the number of current control circuits.

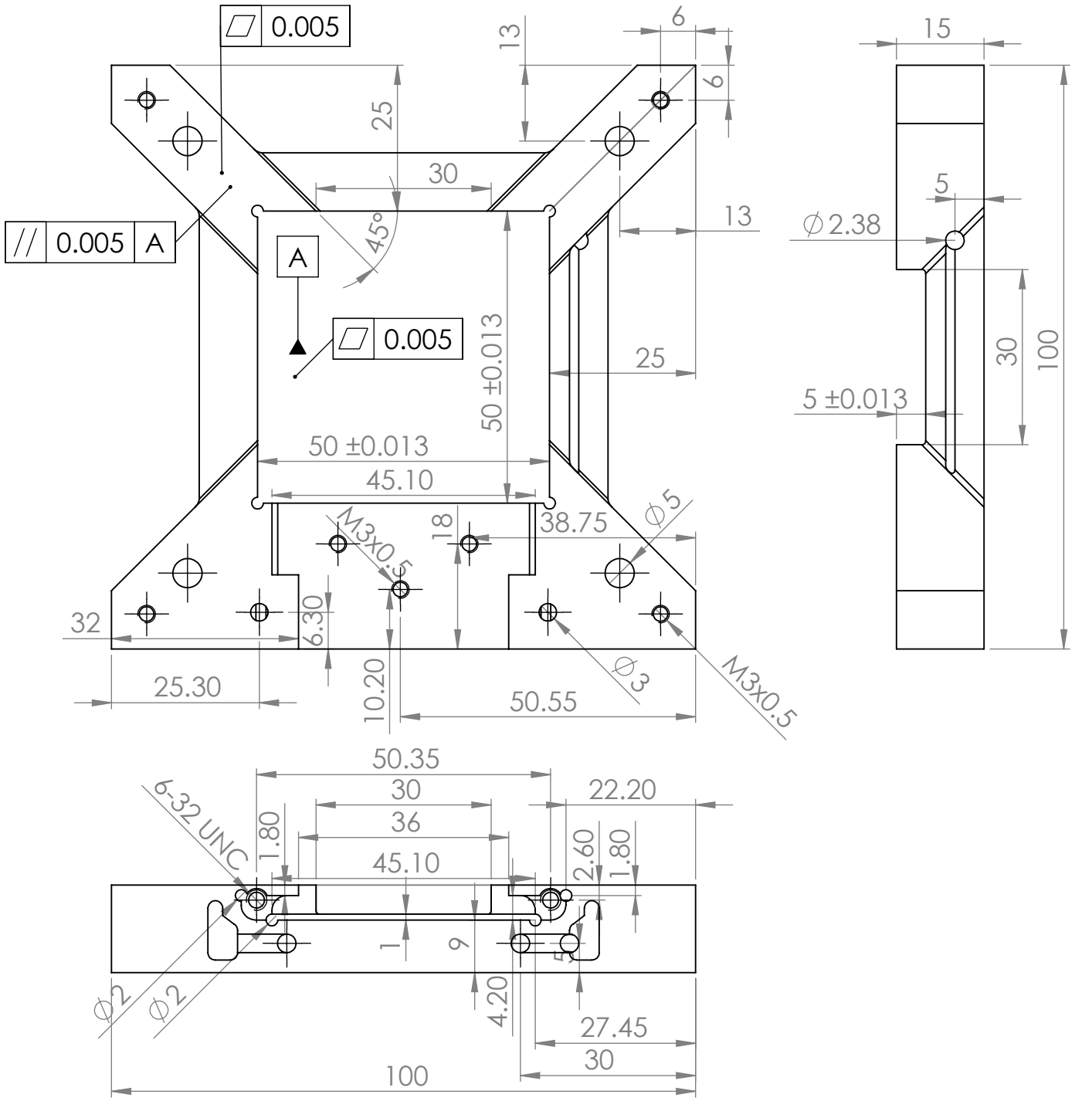
Kaiam will also require a new diode inspection environment that can accommodate the assembly and verify which diodes pass the burn-in. This test rig should take advantage of the shorting connector in order to continue to eliminate the need for a human to interact directly with the CoCs. It will also require a new control board with even tighter tolerancing for the temperature control loop. This second board should be easier to produce since the components do not need to be as heat resistant as they will be in use for shorter amounts of time and in open air.

# 6 Conclusion

This report has discussed the design of a burn-in system for laser diodes. This design meets the objective of the project which is to limit human interaction in the burn-in process and increase throughput of burn-in. It does so by making use of silicon wafers with MEMS cantilevers to make electrical contact with the diodes. These wafers are encased in an aluminum shell with a connector for the traces from the wafer that protects against ESD events. This burn-in solution can be assembled by Kaiam's MRSI machine. The solution costs $376.26 per CoC less than the system currently in place for burn-in. Temperature and current control circuitry have been implemented, and their performance has been tested to meet the specifications for the project. The circuits maintain the temperature of the diodes at $(150 \pm 3)\,^{\circ}\mathrm{C}$ and the current through diodes at $(150 \pm 3)\,\mathrm{mA}$. An enclosure has been designed and simulated to house these components at the appropriate temperatures and to provide cabling and connectivity solutions for the system. Finally, a python library has been created that provides the link between the results from the control board and a human operator. This adds an element of UI to provide a clean interface for those looking to find out information about the burn-in processes currently running while also allowing operators to add new fully loaded shells into the system and start the burn-in. Design details and system usage instructions can be found in the appendices.

# A Mechanical Drawings

This appendix contains the drawings for all of the machined pieces of this project. First the drawings for the bottom shell are included; then, the drawings for the top shell. Finally, a diagram of the shells in the bottom of the enclosure drawer is included.

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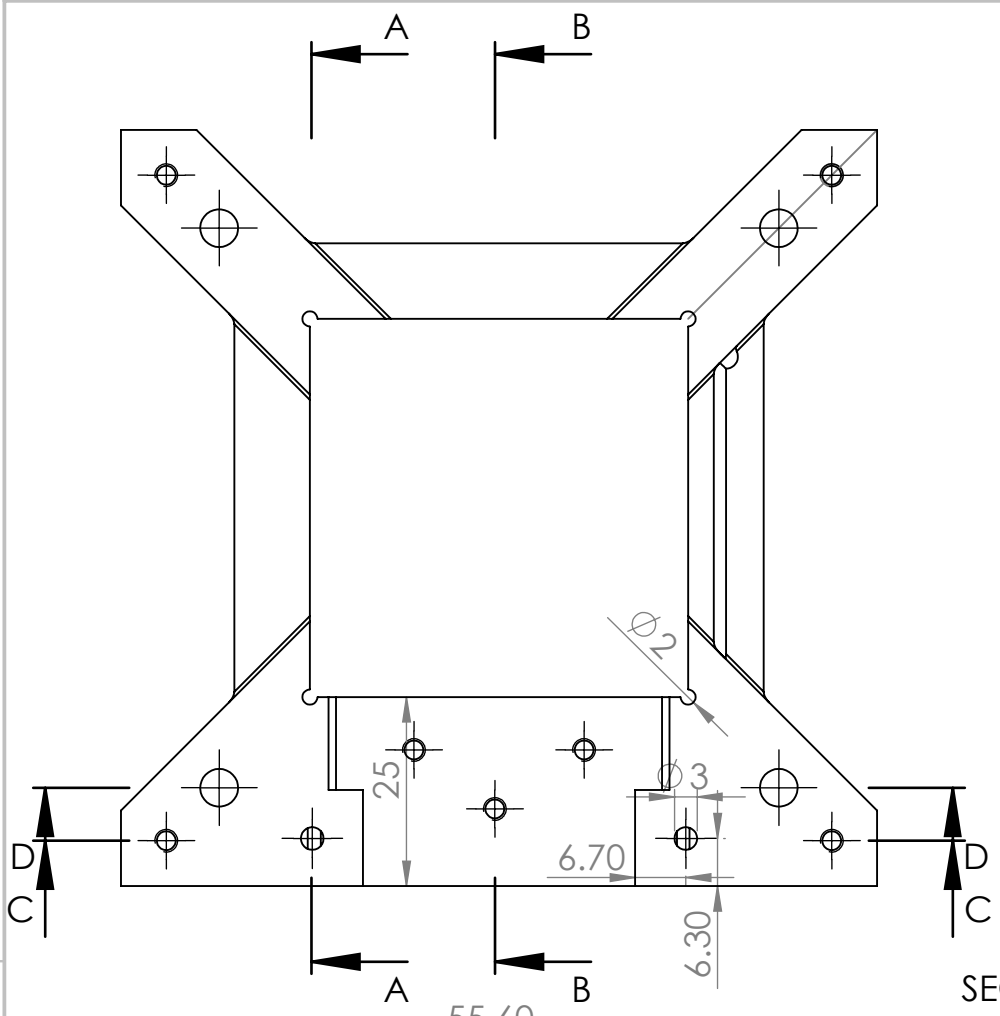
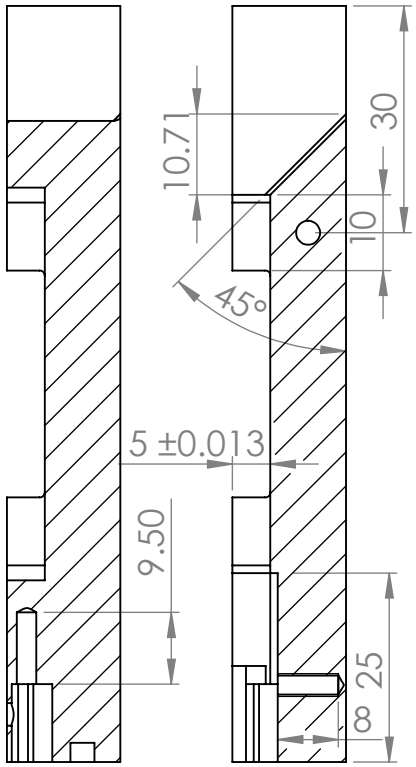
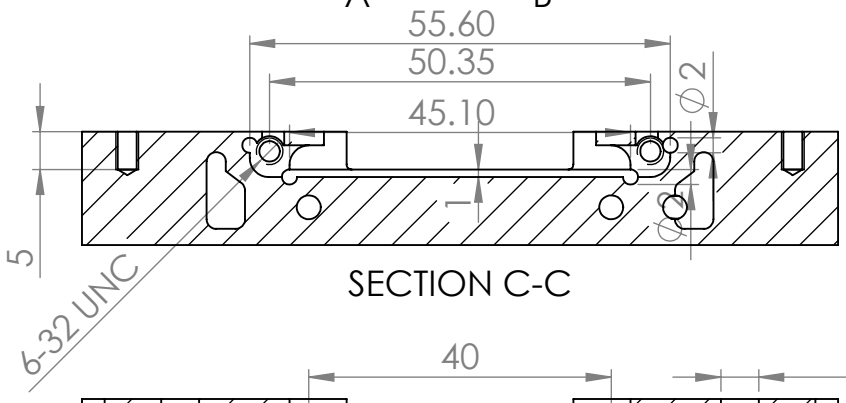
| SIZE | DWG. NO. | REV. |
|---|---|---|
| A | BottomShell_Square210 | |
| SCALE:1:1 | WEIGHT: | SHEET 1 OF 3 |

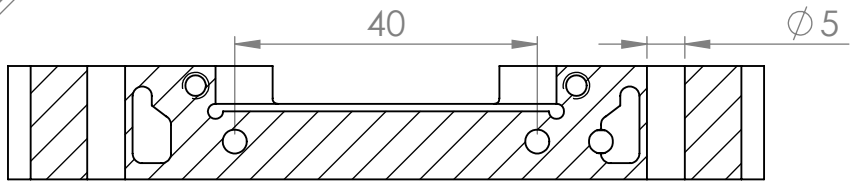



SECTION A-A SECTION B-B




SECTION C-C

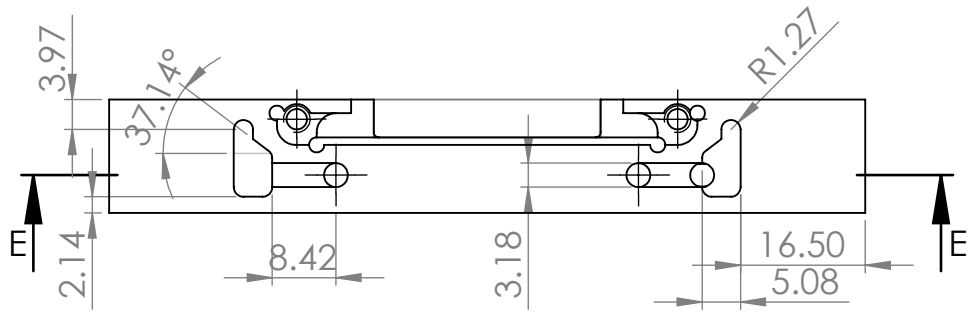


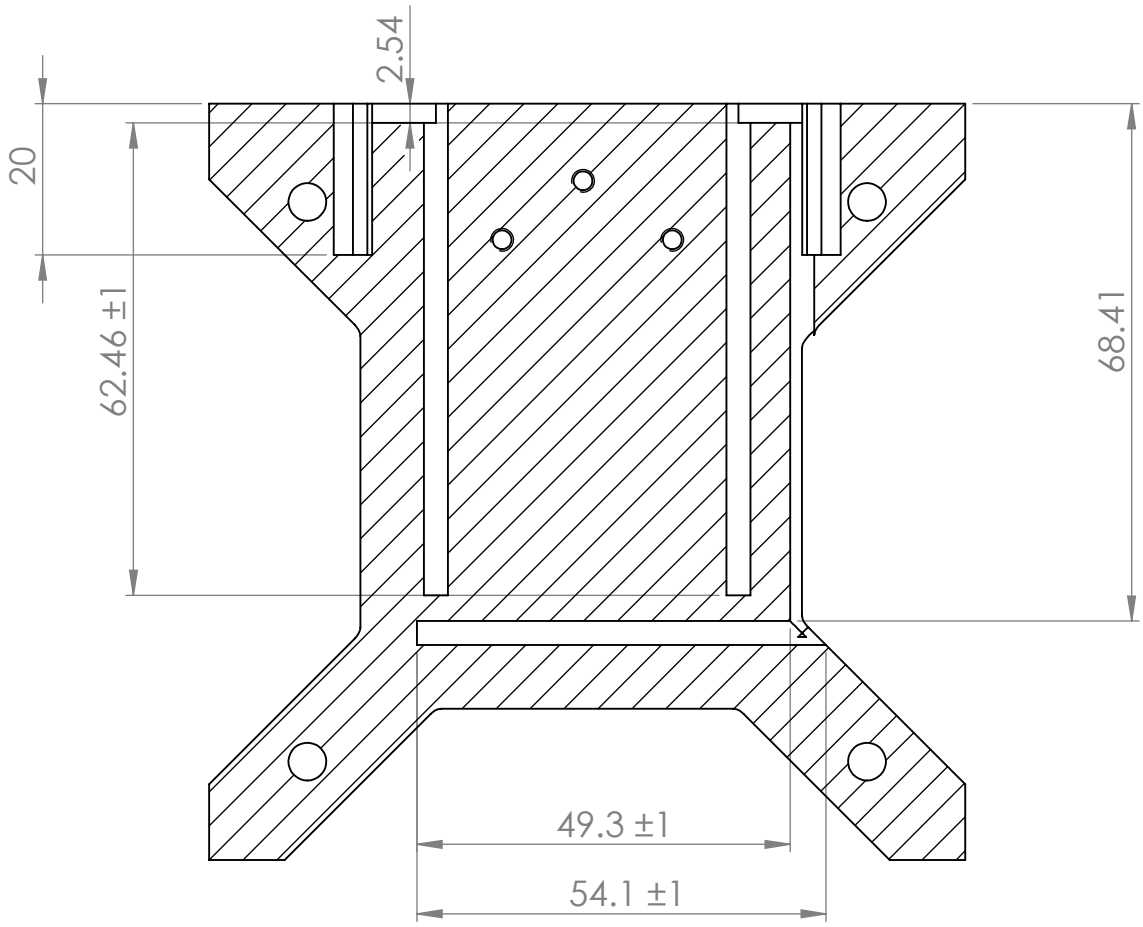

SECTION D-D

| | | | | | |
|---|---|---|---|---|---|
| | | DIMENSIONS ARE IN MM<br>UNLESS OTHERWISE MARKED<br>ALL TOLERANCES ARE: ±0.1 | | NAME | DATE |
| | | | DRAWN | | |
| | | | CHECKED | | |
| | | | ENG APPR. | | |
| | | | MFG APPR. | | |
| | | MATERIAL | Q.A. | | |
| | | | COMMENTS: | | |
| NEXT ASSY | USED ON | FINISH | | | |
| APPLICATION | | DO NOT SCALE DRAWING | | | |



| SIZE | DWG. NO. | REV. |
|---|---|---|
| A | BottomShell_Square210 | |
| SCALE:1:1 | WEIGHT: | SHEET 2 OF 3 |



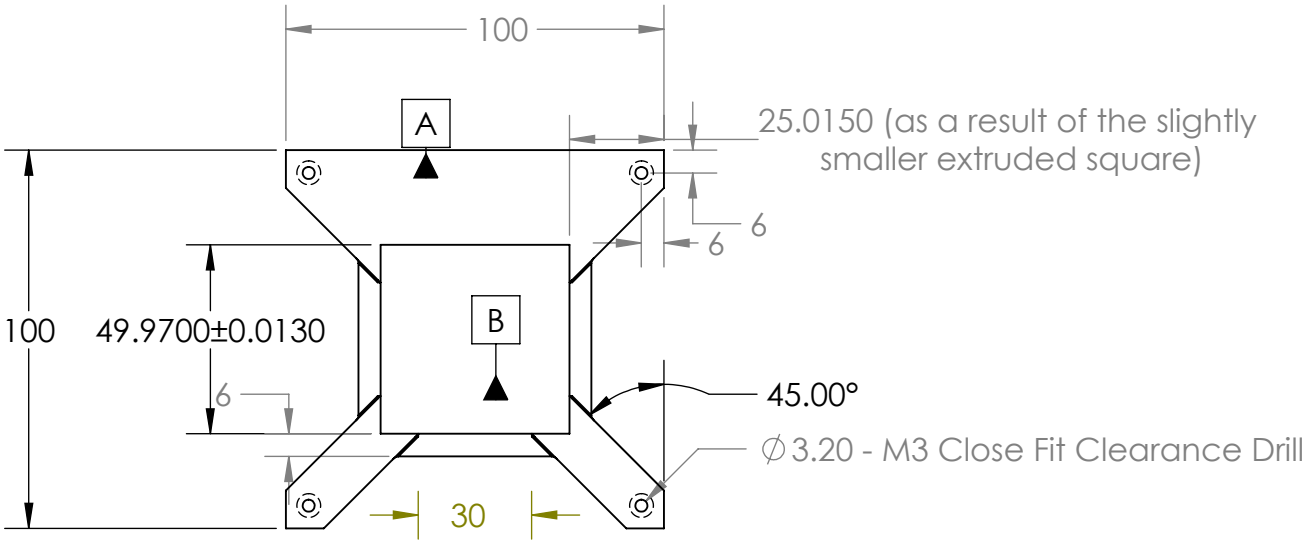



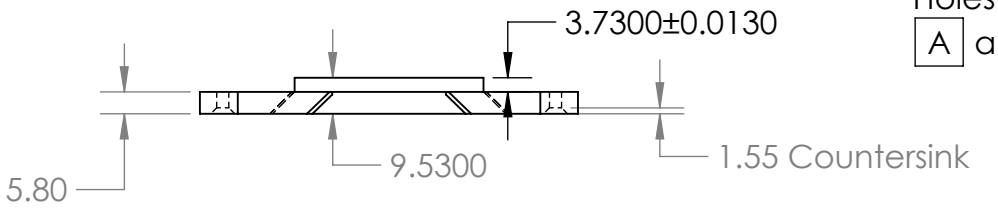

SECTION E-E

| | | | | | |
|---|---|---|---|---|---|
| | | DIMENSIONS ARE IN INCHES<br>TOLERANCES:<br>FRACTIONAL ±<br>ANGULAR: MACH ± BEND ±<br>TWO PLACE DECIMAL ±<br>THREE PLACE DECIMAL ± | | NAME | DATE |
| | | | DRAWN | | |
| | | | CHECKED | | |
| | | | ENG APPR. | | |
| | | | MFG APPR. | | |
| | | MATERIAL | Q.A. | | |
| | | | COMMENTS: | | |
| NEXT ASSY | USED ON | FINISH | | | |
| APPLICATION | | DO NOT SCALE DRAWING | | | |



| SIZE | DWG. NO. | REV. |
|---|---|---|
| A | BottomShell_Square210 | |
| SCALE:1:1 | WEIGHT: | SHEET 3 OF 3 |



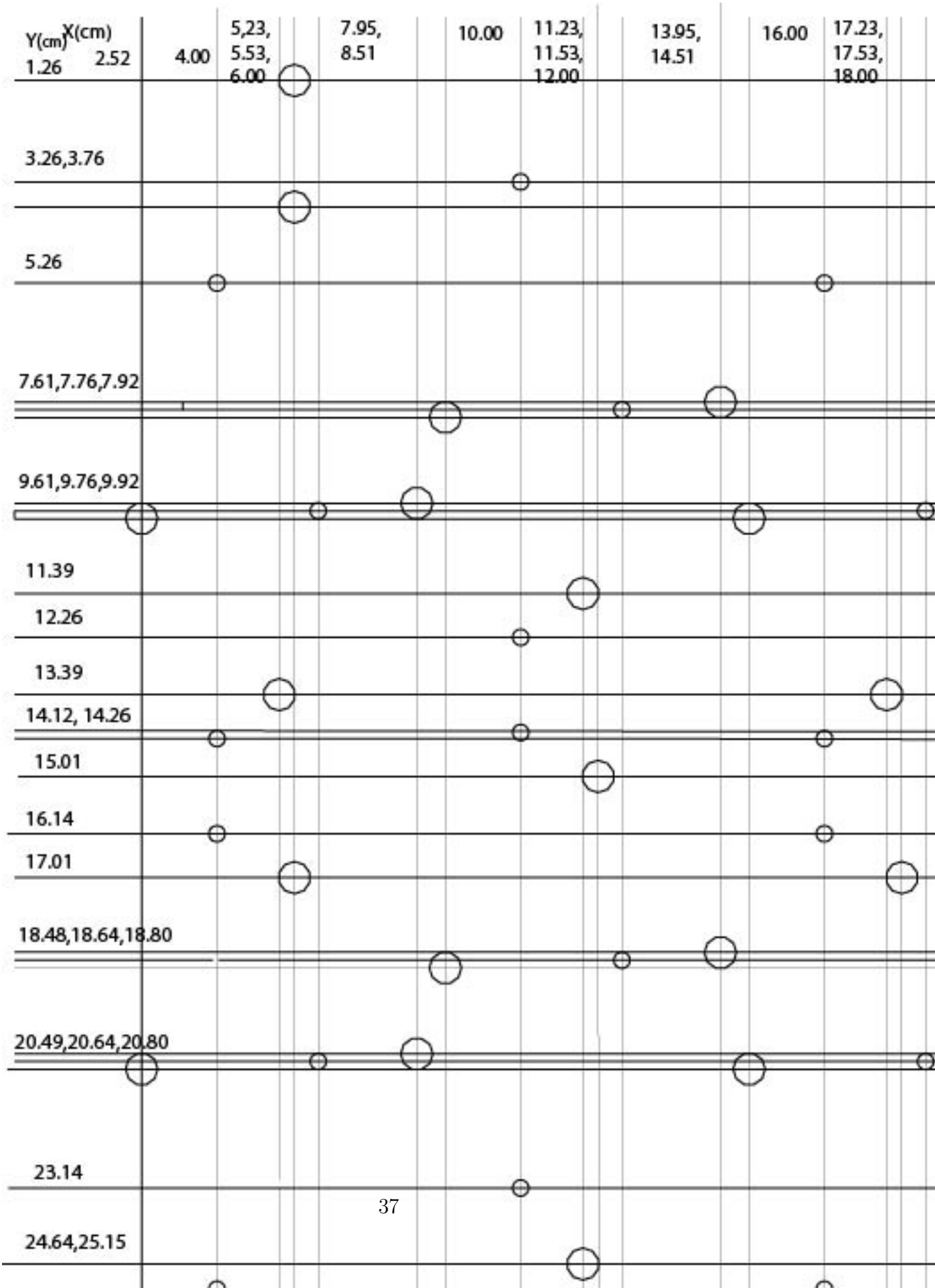

All chamfers are 45 deg.
Fillet radius doesn't matter.
Holes are not tapped.
A and B should be as flat and parallel as possible

| | | | | | |
|---|---|---|---|---|---|
| | | UNLESS OTHERWISE SPECIFIED: | | NAME | DATE |
| | | DIMENSIONS ARE IN MM<br>UNLESS OTHERWISE NOTED<br>TOLERANCES ARE: ± .1 | DRAWN | | |
| | | | CHECKED | | |
| | | | ENG APPR. | | |
| | | | MFG APPR. | | |
| | | INTERPRET GEOMETRIC TOLERANCING PER: | Q.A. | | |
| | | MATERIAL | COMMENTS: | | |
| NEXT ASSY | USED ON | FINISH | | | |
| APPLICATION | | DO NOT SCALE DRAWING | | | |



TITLE:

| SIZE | DWG. NO. | REV |
|---|---|---|
| A | TopShell_Final | |
| SCALE: 1:2 | WEIGHT: | SHEET 1 OF 1 |


Y(cm) X(cm)
1.26
2.52
4.00
5,23,
5.53,
6.00
7.95,
8.51
10.00
11.23,
11.53,
12.00
13.95,
14.51
16.00
17.23,
17.53,
18.00
3.26,3.76
5.26
7.61,7.76,7.92
9.61,9.76,9.92
11.39
12.26
13.39
14.12, 14.26
15.01
16.14
17.01
18.48,18.64,18.80
20.49,20.64,20.80
23.14
24.64,25.15

# B Bill of Materials and Cost Estimate

This appendix contains the complete cost estimate of the burn-in system with links to all of the parts used or recommended. The first page contains an overall BOM and the second contains the BOM for just the combined controller PCB.

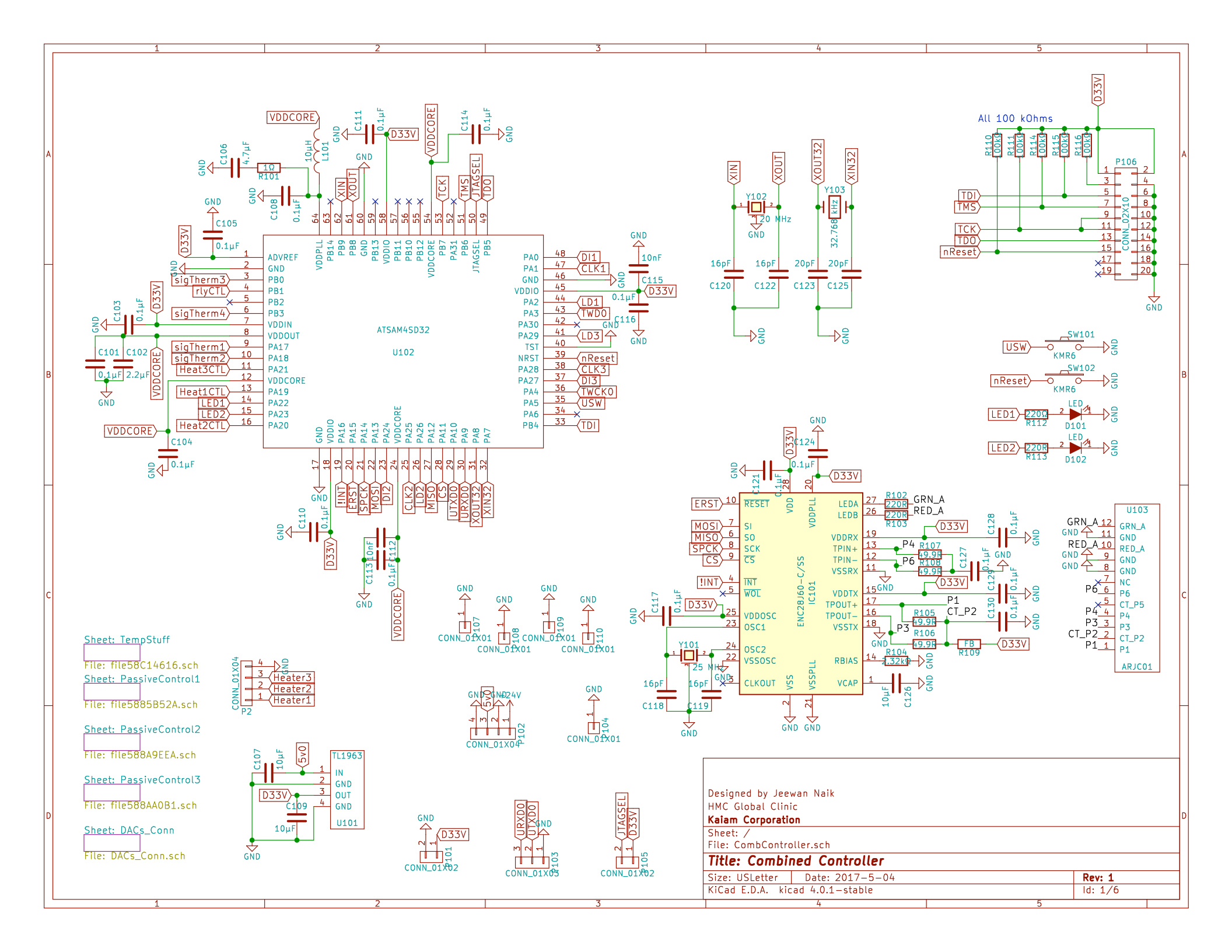
| Name | Quantity Per Drawer | Link | Cost Per Unit | Cost Per Drawer | Value | Notes | | Total Per CoC | |
|---|---|---|---|---|---|---|---|---|---|
| Silicon Wafers | 10 | | $ 1,000.00 | $ 10,000.00 | | Manufactured by Kaiam | | **$ 104.59** | |
| Thermistors | 40 | http://www.mouser.com | $ 3.26 | $ 130.40 | 103FT1005A5P1 | For 1000 units | | | |
| Sapphire Balls | 40 | http://www.swissjewel.c | $ 2.40 | $ 96.00 | 200um | For 1000 units. If we use the next diameter, cost goes down to 75c/unit | | | |
| Male PCIe PCB | 10 | Appendix C | $ 0.15 | $ 1.50 | | For 500 units | | | |
| Shroud PCB | 10 | Appendix C | $ 0.08 | $ 0.84 | | For 500 units | | | |
| Shroud Teeth | 320 | https://www.digikey.con | $ 0.15 | $ 47.53 | 1565322-1 | For 2500 units | | | |
| Screws: Male PCIe PCB | 30 | | $ 0.00 | $ 0.03 | M3-0.5 x 10 mm | For 10k units | | | |
| Shroud Plungers | 20 | https://www.mcmaster.c | $ 3.95 | $ 79.00 | 3126A2 | | | | |
| Shroud Pegs | 20 | http://www.alibaba.com | $ 0.01 | $ 0.20 | | For 100 units | | | |
| Shell | 10 | | $ 240.00 | $ 2,400.00 | | For 500 units | | | |
| Cartridge Heaters | 30 | https://www.comstatinc. | $ 39.20 | $ 1,176.00 | MCH2-80W-001 | | | | |
| Screws: Shell | 40 | | $ 0.00 | $ 0.04 | M3-0.5 x 10 mm | For 10k units | | | |
| Female PCIe PCB | 10 | Appendix C | $ 0.54 | $ 5.38 | | For 500 units | | | |
| 64-pin Connector | 10 | https://www.digikey.con | $ 0.51 | $ 5.10 | Vetical & Keyed | | | | |
| 64-pin Connector Cable | 10 | https://www.digikey.con | $ 1.23 | $ 12.30 | | | | | |
| Mini PCIe Connector | 10 | https://www.digikey.con | $ 0.36 | $ 3.55 | 10018784-10201TLF | For 500 units | | | |
| Nylon Power Connector | 10 | https://www.digikey.con | $ 0.45 | $ 4.50 | M20-7820346 | For 500 units | | | |
| Vertical Headers | 10 | https://www.digikey.con | $ 0.08 | $ 0.84 | M20-9990345 | For 500 units | | | |
| Female PCB Standoffs | 30 | http://www.alibaba.com | $ 0.01 | $ 0.30 | | For 10k units | | | |
| Female PCB Standoff Nuts | 30 | | $ 0.00 | $ 0.03 | | For 10k units | | | |
| L-Brackets | 40 | http://www.alibaba.com | $ 0.10 | $ 4.00 | 2.5" L1, 1" L2, .75" W | Customizeable | | | |
| Bolts: L-Brackets + Rack | 72 | | $ 0.00 | $ 0.07 | 1/4" T-.75" L | For 10k units | | | |
| Nuts: L-Brackets + Rack | 72 | | $ 0.00 | $ 0.07 | 1/4" | For 10k units | | | |
| Washers: L-Brackets + Rack | 72 | | $ 0.00 | $ 0.07 | 1/4" | For 10k units | | | |
| Ceramic Fiber Insulation | 1 | https://www.amazon.co | $ 49.99 | $ 49.99 | | Needs to be cut into shape | | | |
| Rubber Gasket for Insulation | 1 | https://www.amazon.co | $ 32.79 | $ 32.79 | | Needs to be cut into shape | | | |
| Control PCB Standoffs | 48 | http://www.alibaba.com | $ 0.01 | $ 0.48 | | For 10k units | | | |
| Control PCB Standoff Nuts | 16 | | $ 0.00 | $ 0.02 | | For 10k units | | | |
| Screws: Control PCB | 16 | | $ 0.00 | $ 0.02 | M3-0.5 x 10 mm | For 10k units | | | |
| Control PCB | 10 | Appendix C | $ 79.08 | $ 790.80 | | See control PCB breakdown for component details | | | |
| 4U Drawer | 1 | https://www.amazon.co | $ 59.95 | $ 59.95 | | | | | |
| Fan Controller | 0.125 | https://www.newegg.co | $ 44.83 | $ 5.60 | | | | | |
| Cooling Fans | 0.75 | https://www.newegg.co | $ 29.99 | $ 22.49 | AFB1212GHE | 6 fans divided by 8 drawers per rack | | | |
| 12V & 5V Power Supply | 1 | https://www.amazon.co | $ 60.00 | $ 60.00 | | 1 1000W Computer PSU per drawer | | | |
| High Temp Ethernet Cable | 0.125 | http://www.tpcwire.com | $ 3,990.00 | $ 498.75 | | 500ft of heat resistant TPC wire | | | |
| 20 AWG High Temp Cable | 0.5 | https://www.grainger.co | $ 246.50 | $ 123.25 | | 250ft spool | | | |
| 42U Rack | 0.125 | https://www.lonestarrac | $ 299.99 | $ 37.50 | | 1 rack with 8 drawers | | | |
| Ethernet Switch | 0.25 | https://www.amazon.co | $ 121.00 | $ 30.25 | | | | | |
| Thermal Paste | 1 | https://www.amazon.co | $ 8.44 | $ 8.44 | | | | | |

| Quantity | Name | Digikey Part # | Digikey Price | Extended Price | Designator |
|---|---|---|---|---|---|
| 1 | Heater Conn | G88MPB04002C1EU-ND | 0.528 | 0.528 | P2 |
| 8 | 0.1 uF | | 0.02 | 0.16 | C304,C202,C204,C206,C302,C306,C402,C404 |
| 3 | BH2221FV | BH2221FV-E2TR-ND | 1.78 | 5.34 | U501,U503,U502 |
| | | | | | R301,R358,R357,R360,R428,R429,R403,R359,R401,R402,R430,R238,R201,R202,R203,R204,R205,R206,R219,R220,R221,R222,R223,R |
| | | | | | 224,R237,R239,R240,R241,R242,R255,R256,R257,R258,R259,R260,R302,R303,R304,R305,R306,R319,R320,R321,R322,R323,R324,R3 |
| 61 | 100 kΩ | | 0.02 | 1.22 | 37,R338,R339,R340,R341,R342,R355,R356,R410,R411,R412,R419,R420,R421,R9 |
| 4 | Shunt | | 0.02 | 0.08 | R1,R4,R5,R6 |
| 1 | ARJC01 | BH2221FV-E2TR-ND | 1.57 | 1.57 | U103 |
| 4 | Screw Holes | | 0.02 | 0.08 | P108,P107,P109,P110 |
| | | | | | RLY402,RLY206,RLY201,RLY202,RLY203,RLY204,RLY205,RLY301,RLY302,RLY303,RLY304,RLY305,RLY306,RLY401,RLY403,RLY1,RLY2,RLY |
| 18 | 2-1462039-9 | PB1165TR-ND | 2.07 | 37.26 | 3 |
| 6 | Spare DAC Ch | | 0.02 | 0.12 | P505,P506,P501,P502,P503,P504 |
| | | | | | C1, |
| 24 | 0.1 µF | | 0.02 | 0.48 | C505,C506,C501,C101,C103,C104,C105,C108,C110,C111,C113,C114,C116,C117,C121,C124,C127,C128,C129,C130,C502,C503,C504 |
| 18 | Si1032R | SI1032R-T1-GE3TR-ND | 0.11 | 1.98 | Q218,Q213,Q214,Q215,Q216,Q217,Q313,Q314,Q315,Q316,Q317,Q318,Q407,Q408,Q409,Q1,Q2,Q3 |
| 9 | OPA1664 | 296-35039-2-ND | 1.24 | 11.16 | U303,U301,U201,U202,U203,U302,U401,U402,U1 |
| | | | | | C215,C207,C208,C209,C210,C211,C212,C213,C214,C216,C217,C218,C307,C308,C309,C310,C311,C312,C313,C314,C315,C316,C317,C3 |
| 30 | 120 pF | | 0.02 | 0.6 | 18,C405,C406,C407,C408,C409,C410 |
| 1 | 2.2 µF | | 0.02 | 0.02 | C102 |
| 1 | 4.7 µF | | 0.02 | 0.02 | C106 |
| 2 | 10 nF | | 0.02 | 0.04 | C112,C115 |
| 4 | 16 pF | | 0.02 | 0.08 | C118,C119,C120,C122 |
| 2 | 20 pF | | 0.02 | 0.04 | C123,C125 |
| 12 | 10 µF | | 0.02 | 0.24 | C2,C201,C203,C205,C301,C303,C305,C401,C403,C107,C109,C126 |
| 5 | LED | 475-1410-1-ND | 0.04 | 0.2 | D101,D102,D4,D5,D6 |
| 18 | 1N4148WS | 1N4148WSFSTR-ND | 0.03 | 0.54 | D201,D202,D203,D204,D205,D206,D301,D302,D303,D304,D305,D306,D401,D402,D403,D1,D2,D3 |
| 1 | ENC28J60-C/SS | ENC28J60T-I/SSTR-ND | 2.43 | 2.43 | IC101 |
| 1 | 10 µH | | 0.03 | 0.03 | L101 |
| 2 | 2 Pin Conn | S1211EC-20-ND | 0.05 | 0.1 | P101,P105 |
| 1 | UART Conn | S1211EC-20-ND | 0.08 | 0.08 | P103 |
| 1 | GND Pin | S1211EC-20-ND | 0.03 | 0.03 | P104 |
| 1 | JTAG Conn | ED10524-ND | 0.22 | 0.22 | P106 |
| | | | | | Q201,Q202,Q203,Q204,Q205,Q206,Q207,Q208,Q209,Q210,Q211,Q212,Q301,Q302,Q303,Q304,Q305,Q306,Q307,Q308,Q309,Q310, |
| 30 | DMN65 | DMN65D8L-7DICT-ND | 0.03 | 0.9 | Q311,Q312,Q401,Q402,Q403,Q404,Q405,Q406 |
| 1 | 1 Ω | | 0.02 | 0.02 | R101 |
| 5 | 220 Ω | | 0.02 | 0.1 | R102,R103,R113,R14,R15 |
| 1 | 2.32 kΩ | | 0.02 | 0.02 | R104 |
| 4 | 49.9 Ω | | 0.02 | 0.08 | R105,R106,R107,R108 |
| 1 | Ferrite Bead | | 0.14 | 0.14 | R109 |
| 5 | 100kΩ | | 0.02 | 0.1 | R110,R111,R114,R115,R116 |
| 2 | 220Ω | | 0.02 | 0.04 | R112,R13 |
| | | | | | R2, R3, R7, |
| | | | | | R8,R207,R208,R209,R210,R211,R212,R225,R226,R227,R228,R229,R230,R231,R232,R233,R234,R235,R236,R249,R250,R251,R252,R25 |
| | | | | | 3,R254,R307,R308,R309,R310,R311,R312,R325,R326,R327,R328,R329,R330,R331,R332,R333,R334,R335,R336,R349,R350,R351,R352, |
| 63 | 1 kΩ | | 0.02 | 1.26 | R353,R354,R404,R405,R406,R413,R414,R415,R416,R417,R418,R425,R426,R427 |
| | | | | | R213,R214,R215,R216,R217,R218,R243,R244,R245,R246,R247,R248,R313,R314,R315,R316,R317,R318,R343,R344,R345,R346,R347,R |
| 30 | 0.1 Ω | | 0.02 | 0.6 | 348,R407,R408,R409,R422,R423,R424 |
| 2 | KMR6 | CKN10684TR-ND | 0.15 | 0.3 | SW101,SW102 |
| 1 | TL1963 | 296-24897-2-ND | 1.24 | 1.24 | U101 |
| 1 | ATSAM4SD32 | ATSAM4SD32BA-AU-ND | 6.92 | 6.92 | U102 |
| 1 | 32.768 kHz | 535-12373-2-ND | 0.36 | 0.36 | Y103 |
| 1 | 25 MHz | 535-10941-2-ND | 0.77 | 0.77 | Y101 |
| 1 | 20 MHz | 535-10939-2-ND | 0.67 | 0.67 | Y102 |
| 1 | Ribbon Conn | ED10532-ND | 0.51 | 0.51 | P1 |
| 4 | DNP | | 0.02 | 0.08 | C3,C4,C5,C6 |
| 1 | 27 kΩ | | 0.02 | 0.02 | R10 |
| 1 | Power Conn | WM13410-ND | 0.3 | 0.3 | P102 |
| | | | | 79.078 | |

# C PCB Layout & Schematics

This appendix contains the schematics and layouts for all of the PCBs designed for this project. In order of apperance after this page, the boards are as follows:

1. Combined Controller
2. Shorting Connector
3. Shroud PCB
4. Female PCIe Board
5. Dummy Electrical Wafer




Sheet: TempStuff

File: file58C14616.sch

Sheet: PassiveControl1

File: file5885B52A.sch

Sheet: PassiveControl2

File: file588A9EEA.sch

Sheet: PassiveControl3

File: file588AA0B1.sch

Sheet: DACs_Conn

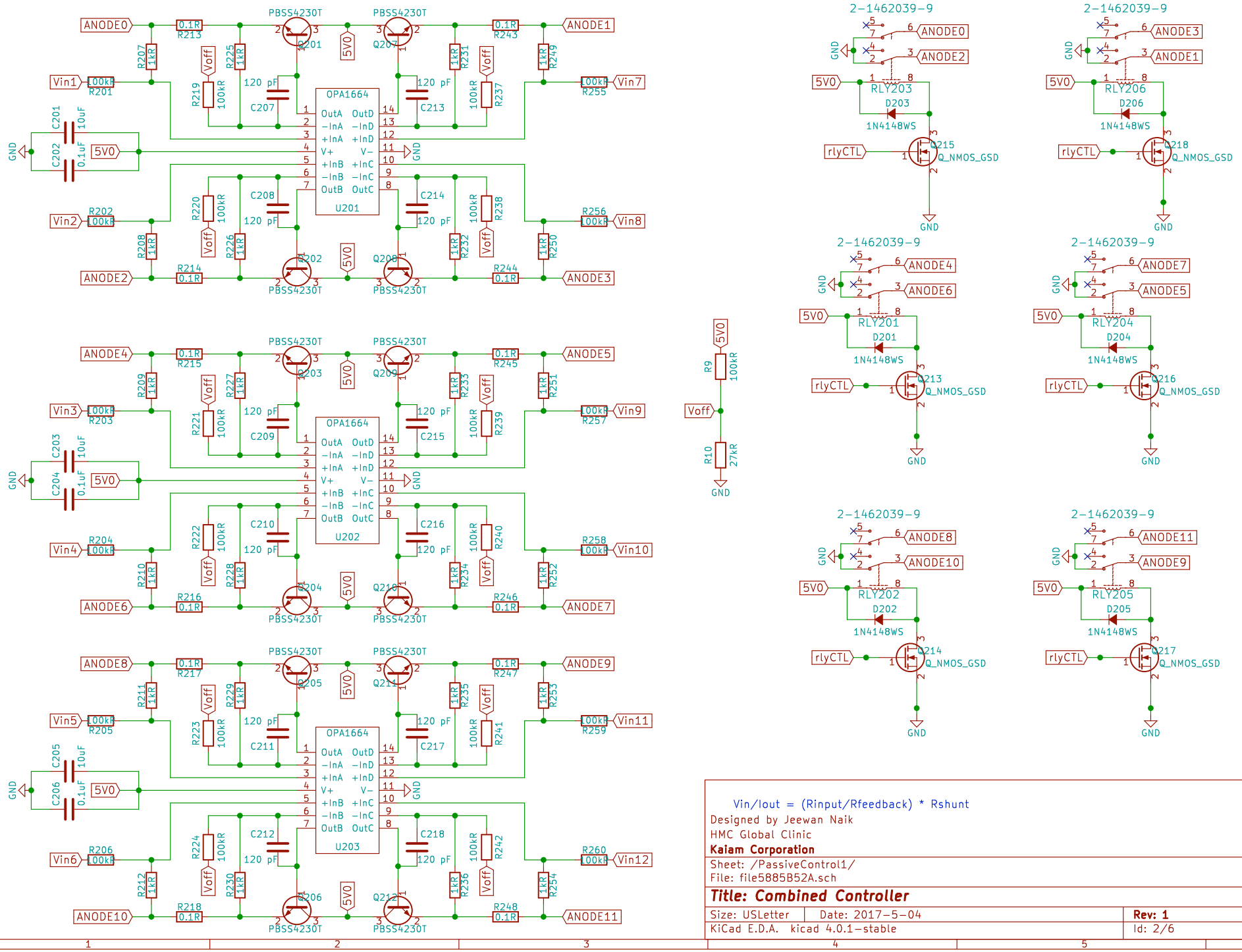
File: DACs_Conn.sch

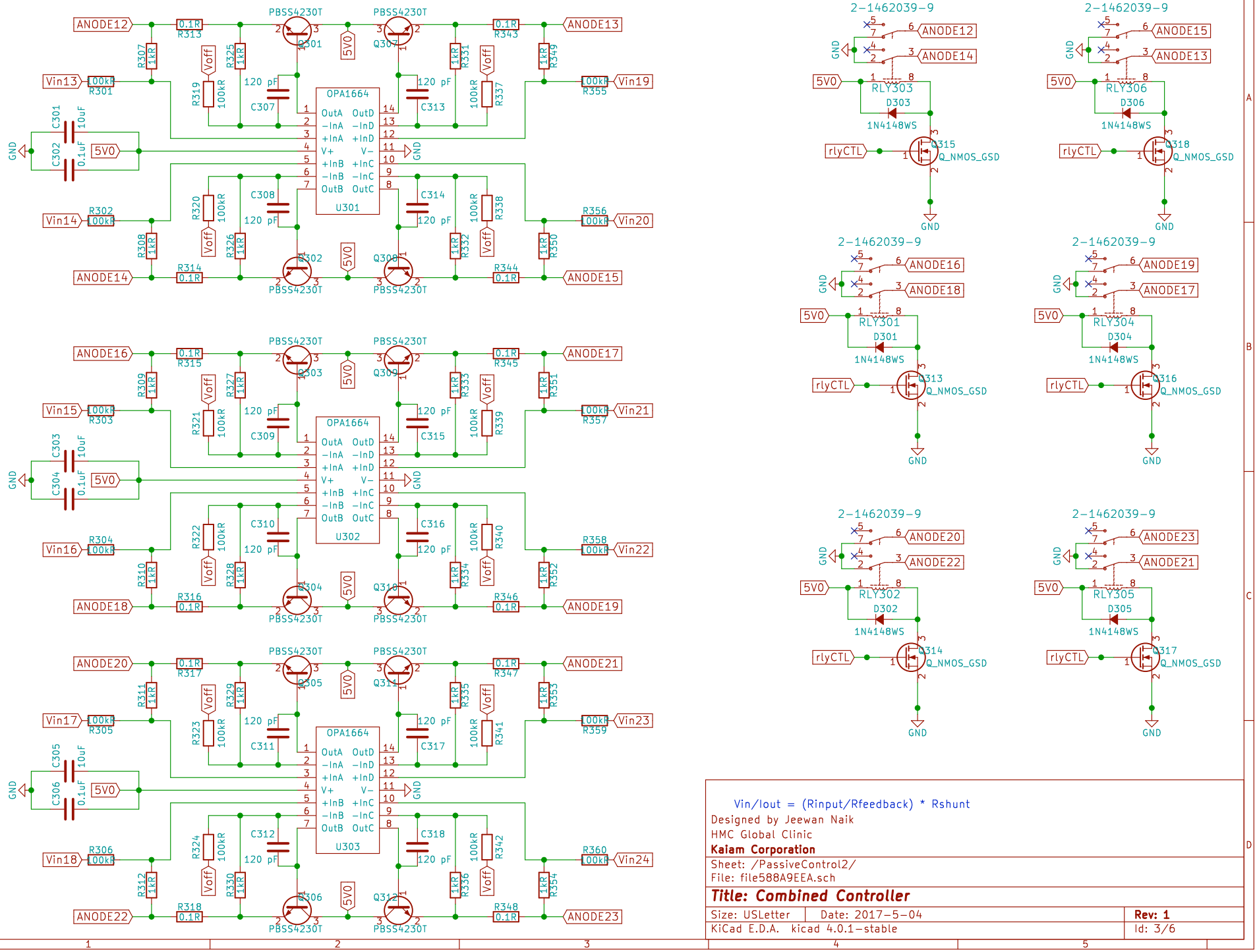
Designed by Jeewan Naik
HMC Global Clinic
**Kaiam Corporation**

Sheet: /
File: CombController.sch

**Title: Combined Controller**

| Size: USLetter | Date: 2017-5-04 | **Rev: 1** |
|---|---|---|
| KiCad E.D.A. kicad 4.0.1-stable | | Id: 1/6 |


ANODE0
ANODE1
ANODE2
ANODE3
ANODE4
ANODE5
ANODE6
ANODE7
ANODE8
ANODE9
ANODE10
ANODE11
Vin1
Vin2
Vin3
Vin4
Vin5
Vin6
Vin7
Vin8
Vin9
Vin10
Vin11
Vin12
PBSS4230T
OPA1664
U201
U202
U203
5V0
GND
Voff
rlyCTL
Q_NMOS_GSD
1N4148WS
2-1462039-9
RLY203
RLY206
RLY201
RLY204
RLY202
RLY205
D203
D206
D201
D204
D202
D205
R9
R10
100kR
27kR
Vin/Iout = (Rinput/Rfeedback) * Rshunt
Designed by Jeewan Naik
HMC Global Clinic
Kaiam Corporation
Sheet: /PassiveControl1/
File: file5885B52A.sch
Title: Combined Controller
Size: USLetter
Date: 2017-5-04
Rev: 1
KiCad E.D.A. kicad 4.0.1-stable
Id: 2/6




Vin/Iout = (Rinput/Rfeedback) * Rshunt

Designed by Jeewan Naik

HMC Global Clinic

**Kaiam Corporation**

Sheet: /PassiveControl2/

File: file588A9EEA.sch

**Title: Combined Controller**

| Size: USLetter | Date: 2017-5-04 | **Rev: 1** |
|---|---|---|
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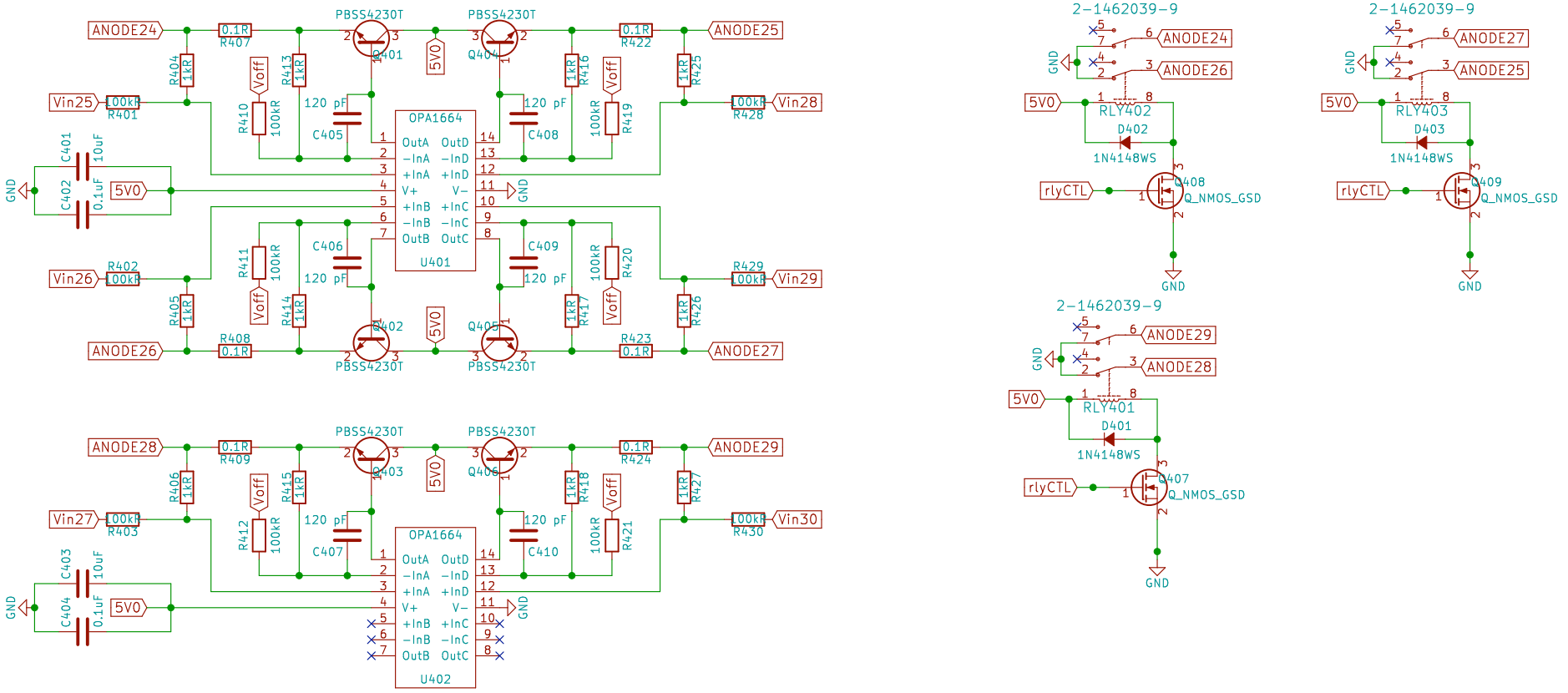


Vin/Iout = (Rinput/Rfeedback) * Rshunt

Designed by Jeewan Naik

HMC Global Clinic

**Kaiam Corporation**

Sheet: /PassiveControl3/

File: file588AA0B1.sch

***Title: Combined Controller***

| Size: USLetter | Date: 2017-5-04 | **Rev: 1** |
|---|---|---|
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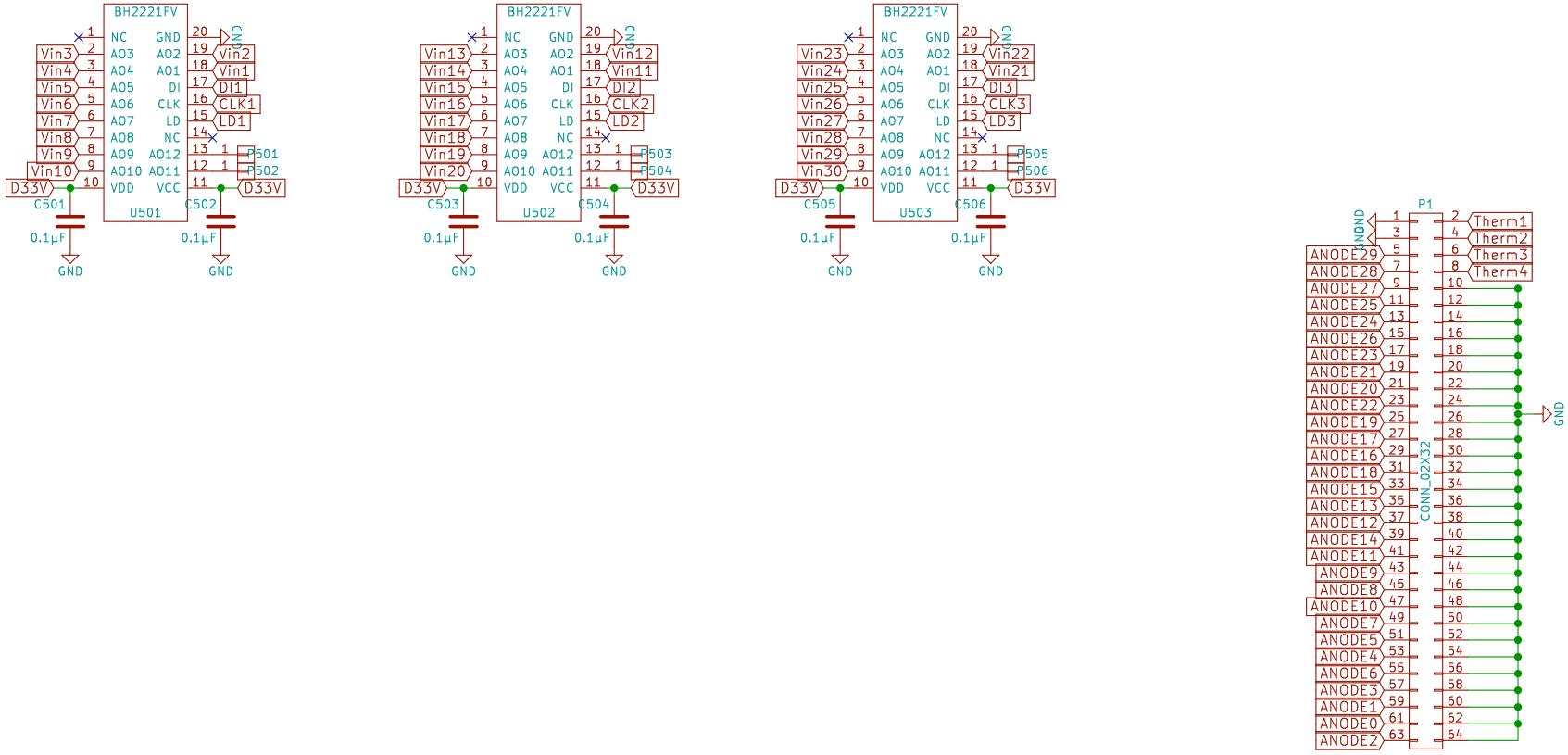


Designed by Jeewan Naik
HMC Global Clinic
**Kalam Corporation**

Sheet: /DACs_Conn/
File: DACs_Conn.sch

***Title: Combined Controller***

| Size: A4 | Date: 2017-5-04 | **Rev: 1** |
|---|---|---|
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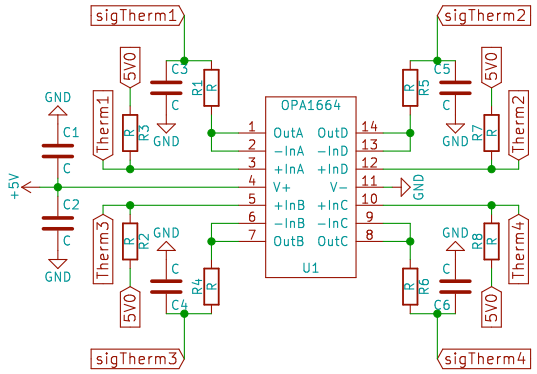


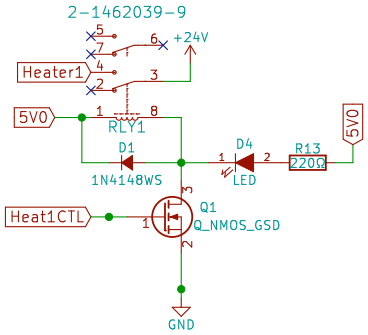


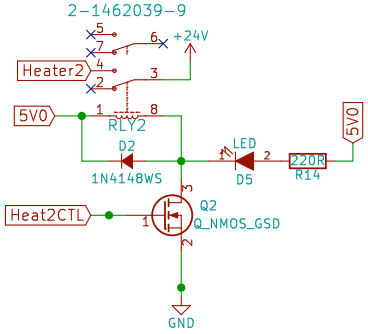


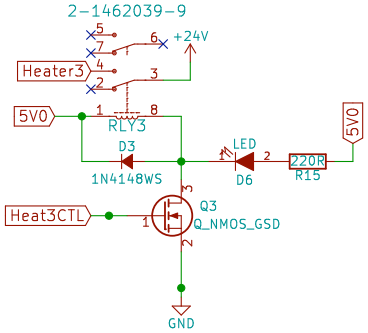


Designed by Jeewan Naik
HMC Global Clinic
**Kalam Corporation**

Sheet: /TempStuff/
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***Title: Combined Controller***

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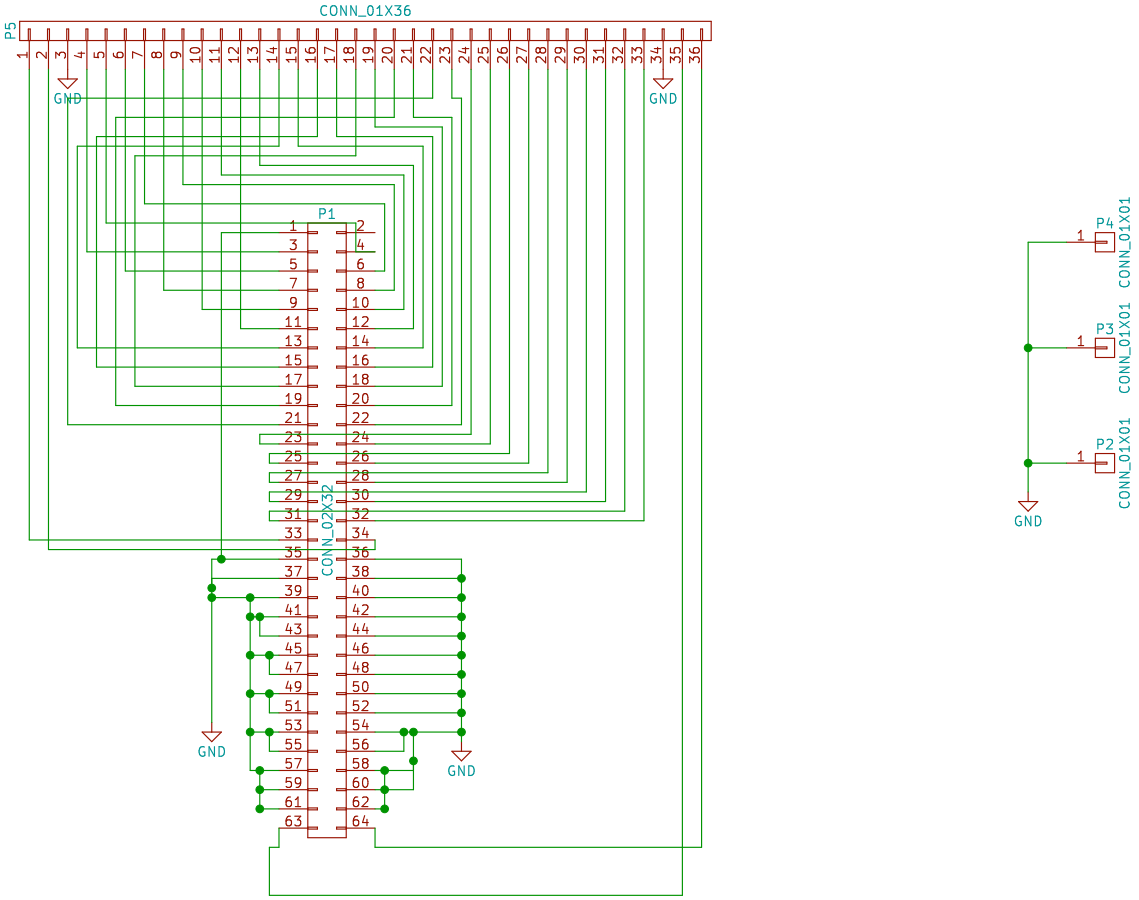





Designed By
Evan Kahn
HMC Global Clinic
**Kaiam**

Sheet: /
File: ShortingConnector.sch

***Title: Shorting Connector***

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|---|---|---|
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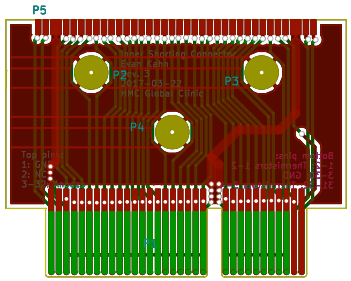


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**Kaiam**

Sheet:
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***Title: Shorting Connector***

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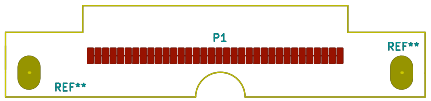


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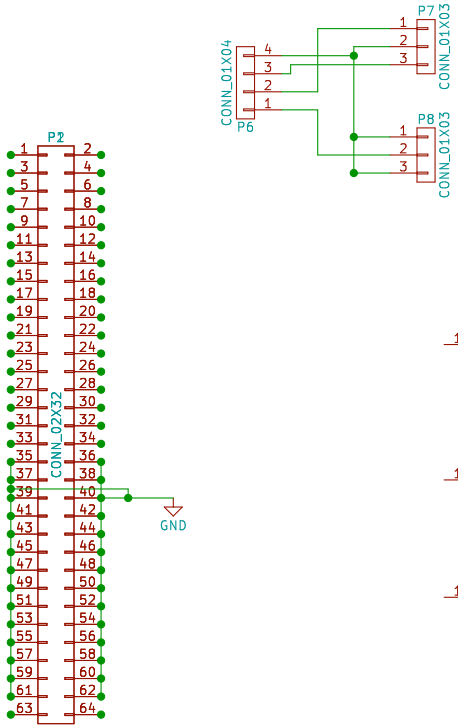


Designed By
Evan Kahn
HMC Global Clinic
**Kaiam**

Sheet: /
File: Female_PCIe.sch

***Title: Female PCIe Breakout***

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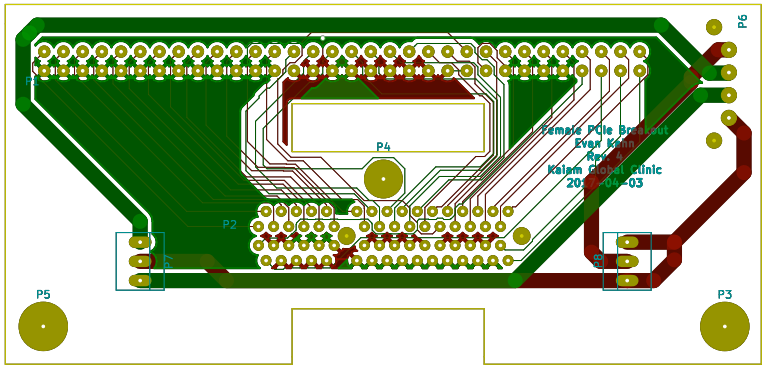


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Sheet:
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***Title: Female PCIe Breakout***

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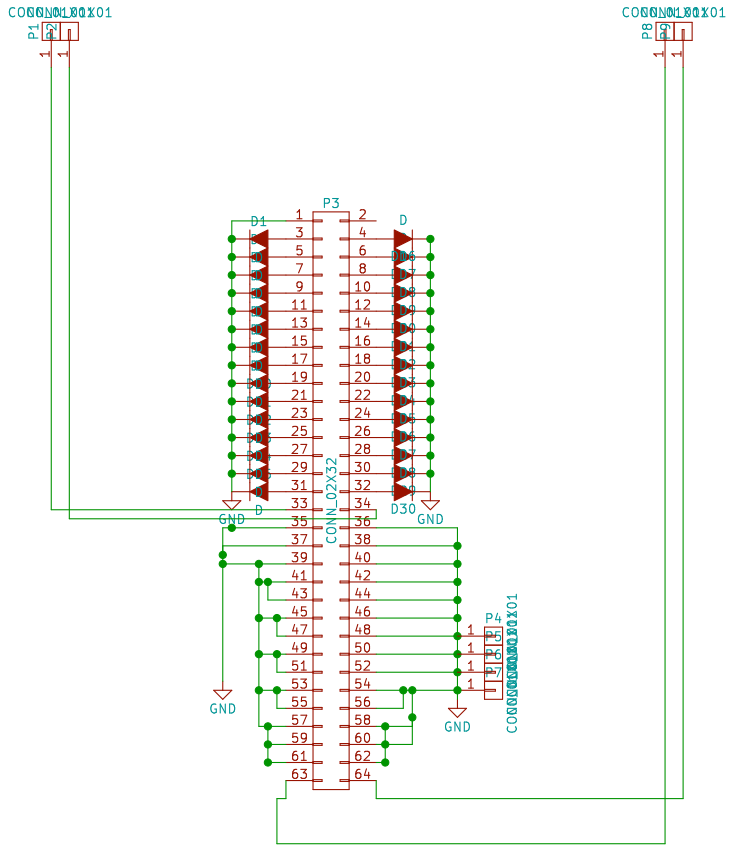


Designed By
Evan Kahn
HMC Global Clinic
**Kaiam**

Sheet: /
File: DummyWafer.sch

***Title: Dummy Wafer***

| Size: A4 | Date: | **Rev:** |
|---|---|---|
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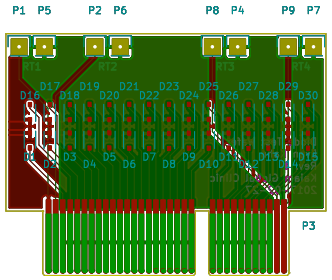


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Sheet:
File: DummyWafer.kicad_pcb

***Title: Dummy Wafer***

| Size: A4 | Date: 5/4/2017 | **Rev: 1** |
|---|---|---|
| KiCad E.D.A. kicad 4.0.5 | | Id: 1/1 |

# D Code

The code for this project includes both the initial development of the python library and also the microcontroller code written in C. The microcontroller was debugged in Keil and the complete Keil packages are availble on the DVDs included with this final report. Besides the content in the main.c file, the system_SAM4S.c file provided by Keil should have line 215 and 216 changed as shown below to set the PLLs to the correct speed.

```
#define CKGR_PLLAR_Val  0x201F0606      // 0x00003F00
#define CKGR_PLLBR_Val  0x00170608      // 0x00003F00
```

The python library code is reproduced below:

```
import csv

mac_db  = 'mac_addrs.csv'
temp_db = 'temp_addrs.csv'

SHELLS_PER_DRAWER = 10
DRAWERS_PER_RACK  = 8

# helper functions for MAC address conversion

def mac_to_str(mac):
    d=''
    for char in mac:
        d += char.encode("hex")
        d += ':'
    return d[0:-1]

def str_to_mac(val):
    a = val.split(':')
    print a
    r = ''
    for e in a:
        r += chr(int(e,16))
    return r

# Shell class

class Shell:
    def __init__(self, mac=-1):
        self.mac = -1 # initialize to no set MAC address
        self.current = 0 # no current set point
        self.temp_cal_recvd = False # has not received temperature
           coefficients
        self.temp_coeffs = [0]*4
        self.connected = False # starts off disconnected

    def get_status(self):
        '''
        possible shell statuses:
```

```
            0: no board (no MAC address on file)
            1: MAC address on file, no communication
            2: MAC address on file, communication
            3: temp coefficients specified, not sent
            4: temp calibration data received
            5: disabled

            shell status tells us what commands are legal to send to a
               given shell.
            note, self.status should ONLY change in this function!
        '''
        if self.mac == -1:
            return 0
        elif self.connected == False:fjhkljhk
            return 1
        elif self.temp_coeffs == []:
            return 2
        elif self.temp_cal_recvd == False:
            return 3

    def set_mac_addr(self, mac):
        self.mac = mac

    def set_current(self, curr):
        self.current = curr

    def set_temp_coeffs(self,code):
        if self.get_status() < 3: return -1 # won't work if temp
           coefficients haven't been loaded from csv file
        with open (temp_db) as csvread:
            reader = csv.DictReader(csvread, fieldnames=['key','tc1','
               tc2','tc3','tc4']) # read out four 16-bit temperature
               calibration values
            for row in reader:
                if code == row['key']:
                    self.temp_coeffs[0] = int(row['tc1'],16)
                    self.temp_coeffs[1] = int(row['tc2'],16)
                    self.temp_coeffs[2] = int(row['tc3'],16)
                    self.temp_coeffs[3] = int(row['tc4'],16)
                    break
            else:
                return -1
        return 1

    def get_temp_coeffs(self):
        return self.temp_coeffs

    def send_command(self, command_type, data=None):
        '''
        first byte: command type
            00: request info (min. status: 1)
            01: send temp. calibration data (min. status: 3)
            02: set temp. (min. status: 4)
            03: set current. (min. status: 4)
```

```
            04: disable. (min. status: 2)
            05: enable. (min. status: 5)
        '''

        # min_status stores the minimum possible executable command for
            each shell status
        min_status = {0:1, 1:3, 2:4, 3:4, 4:2, 5:5}

        packet = chr(command_type)
        try:
            if self.get_status() < min_status[command_type]:
                print "Command failure: status too low! Required status
                    : "+str(min_status[command_type])+"; actual status:
                    "+str(self.get_status())
                return -1
        except:
            print "Command failure: command "+str(command_type)+" not
                found!"
            return -1

        # assemble packet from command type and payload

        packet += data
        if debug: print packet

    def sendeth(src, dst, eth_type, payload, interface = "eth0"):
        # send packet over ethernet to target board
        # currently unimplemented
        # possible lead here? https://gist.github.com/cslarsen/11339448
        pass

    def get_mac_addr(self):
        return self.mac

# object oriented classes for rack, drawer

class Drawer:
    def __init__(self, index):
        self.shells = [Shell() for n in range(SHELLS_PER_DRAWER)]
        self.index = index

    def print_shells(self):
        for s in self.shells: print s.get_status(),
        print ''

    def init_board(self, shell_index, mac):
        self.shells[shell_index].set_mac_addr(mac)
        loc_code = str(self.index) + str(shell_index)
        # if we are adding a new board, put its MAC address into the
            CSV file
        with open (mac_db, 'r') as csvread:
            with open('temp.csv', 'wb') as csvwrite:
                writer = csv.DictWriter(csvwrite, fieldnames=['drawer',
                    'shell','macaddr'])
```

```
                reader = csv.DictReader(csvread, fieldnames=['drawer','
                    shell','macaddr'])
                for row in reader:
                    if row['drawer'] != str(self.index) or row['shell']
                        != str(shell_index):
                        writer.writerow(row)
                writer.writerow({'drawer':str(self.index),'shell':
                    shell_index,'macaddr':mac})
        os.rename('temp.csv',mac_db)

    def add_shell(self, index, temp_coeffs):
        self.shells[index].set_temp_coeffs(temp_coeffs)

    def get_shell(self, index):
        return self.shells[index]

class Rack:
    def __init__(self):
        self.drawers = [Drawer(n) for n in range(DRAWERS_PER_RACK)]
        with open(mac_db) as csvfile:
            reader = csv.DictReader(csvfile, fieldnames=['drawer','
                shell','macaddr'])
            for row in reader:
                drawer_ind = int(row['drawer'])
                shell_ind  = int(row['shell'])
                self.drawers[drawer_ind].get_shell(shell_ind).
                    set_mac_addr(row['macaddr'])

    def print_status(self, index=0):
        for d in self.drawers:
            d.print_shells()

    def get_drawer(self, index):
        return self.drawers[index]
```

# Glossary

**Assembly** The combination of the shell and the wafers when put together.

**Bottom Wafer** The piece of silicon which holds the CoCs and contains the connections to the shorting connector; collectively known as "wafers" with the top wafer.

**Control Board** PCB containing current and temperature control circuitry.

**Enclosure** Structure housing assemblies and control boards.

**Plunger** Metal hardware which includes a spring inside of a screw which pushes a post out of the screw. The shroud rests against this plunger, which provides the restoring force to short the CoCs when they are removed from burn-in rack.

**Rack** Fixture that mounts enclosures/drawers.

**Shell** The outer aluminium casing that holds the two wafers.

**Shorting Connector** PCB that connects together anode and cathode of the diodes to the enclosure wiring. The wafer connections are wire bonded to the shorting connector and then connected to the pads of an edge card connector with the same form factor as mini-PCIe. The edge card pads can be shorted together by the shroud for ESD protection.

**Shroud** Thin PCB which has teeth on it and slides back and forth on top of the shorting connector. The teeth are all electrically connected to short together the anode and cathodes of all CoCs mounted in the shell.

**Top Wafer** The piece of silicon which contains the MEMs probes and makes contact with the CoCs; collectively known as "wafers" with the bottom wafer.